

Urdhva Tiryak Sutra Based Ancient Multiplication in Reversible Logic Circuits



K. Saranya, N. Priya, M. Priyadharshini, D. Vedhanivetha, B. Lukman

Abstract— The proposed work analyses the employment of an ancient mathematical approach for building an arithmetic logic unit. Dissipation of power is one of the major driving issues in VLSI design. With the assistance of reversible gates, the power dissipation and loss of information can be minimized. The speed and accuracy of the Arithmetic Logic Unit depends on the propagator. Employing the traditional mathematics sutras technique within the computation algorithm reduces the complexity, duration and power. Due to the effect of environmental factors on the digital circuits, parity conserving technique is incorporated for providing error detection ability. The proposed work deal with the design and analysis of 32 bit reversible multiplier using ancient sutras with and without parity conserving technique. The planned work is implemented on Xilinx ISE Spartan 6E series of FPGA and simulation results are obtained. By using Cadence EDA tool, power, area and delay are calculated. The quantum parameters are calculated manually for 32-bit reversible multiplier using ancient technique with and without parity conserving technique using Urdhva Tiryakbhyam sutra.

Keywords: Ancient multiplier, ASIC parameters, parity conserving, quantum parameters

I. INTRODUCTION

In the recent years, Reversible logic gates have received great attention thanks to their ability to scale back the dissipation of power which is the most requirements in low power VLSI design. These reversible logic gates support the method of running the system in both direction and might also generate inputs from outputs might pause and return to any point within the computation history. A circuit is alleged to be reversible if the output vector is uniquely recovered from the input vector and vice-versa and has one-to-one correspondence between its input and output assignments. Dissipation of energy is reduced or maybe eliminated if computation becomes information-lossless.

Revised Manuscript Received on March 30, 2020.

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With higher orders of integration and rising scaling mechanism; Moore's law is found to be accurate yet, but in traditional technologies heat produced by each IC doubles.

Conventional logic circuits has temperature reduction in an order of $kT \ln 2$ joules for every bit of information which is lost, where k refers to the Boltzmann constant and T refers to the operating temperature. Reversible logic gates have the foremost advantages and are utilized in CMOS, QCA technologies which consumes low power. It does multiple operations in an exceedingly single cycle. These gates are more adaptable in quantum computing. It is also used to recover bit-loss well as heat production. The mapping of inputs to output is objective. Each input is mapped to unique output and contrariwise. So, reversible computation produces no information loss operation making them best suited choice for QCA nanotechnologies..

Reversible logic difference from irreversible Boolean logic synthesis 5 major ways like:

1. Constant inputs are the inputs which are kept constant either as 1 or 0. The count of constant inputs must be less for an efficient circuit,
2. Fan-out is the possible number of gate input that the output of the logic gate can drive. The single output of a gate can be connected to only one of the inputs.
3. Garbage signals is the output of gate that is not used in the other gate. For an effective circuit, the garbage value must be less.
4. Unlike irreversible circuits, reversible circuits comprises of same number of inputs and outputs. This logic circuit is acyclic, since there is no feedback path.
5. Hardware complexity of defined as the quantity of basic gates, which are used to synthesize the given logic function.

Reversible computation does not produce any loss of information due to the availability of the one to one mapping concept. These types of gates have same number of inputs and outputs. Hence, they can be uniquely retrievable from each other. The inputs can be reconstructed from the outputs without consuming any power. Irreversible gates often dissipate some sort of energy. This type of problem can be solved by using reversible gates. Reversible logic gates have an advantage of zero power dissipation. The speed of operation is also high in reversible gates. Reversible logic are used in different applications such as online and offline testing of faults. Reversible gate is balanced by adding constant inputs and garbage outputs. Constant input is the number of gates which is kept constant to make the gate reversible. Garbage outputs are unused outputs. These outputs are not used by any other inputs; It remains unconnected.



Reversible logic gates can generate both inputs from outputs and outputs from inputs. Evaluation of reversible circuits are based on different c such as garbage outputs, gate count, constant input, latency and hardware complexity.

II. LITERATURE SURVEY

R. Landauer [1] proposed two simple representative and appropriate models of bi-stable devices and is subjected to a more detailed analysis of switching kinetics to obtain the comparison of speed and energy dissipation. He also put forward points about heat dissipation and its importance in standardizing signals. Himanshu Thapliyal [3] and M.B.Srinivas [3] proposed a reversible ancient multiplier incorporating the TSG gate and the intermediate products were generated in correlation with delay employing Fredkin gates and hence, the summation is reduced to $\log_2 N$ steps by using reversible parallel summer.

Vijeyakumar, K.[6], Elango, S.[6] and Kalaiselvi, S.[6] proposed the design of a energy efficient and high speed truncated multiplier which reduces some intermediate product bits and adds correction bias to it to eliminate the total error with the help of ancient sutras to generate intermediate product bits..

Jain,[10] and S. C. Jain[10] proposed new 4 bit parity conserving reversible logic gate called Parity conserving Toffoli Gate and realized it's quantum specifications and utilization of new parity conserving technique allows to employ existing conserving parity with one additional circuitline.

Akbar, E.[12], Haghparast, M.[12] and Navi.[12] in 2012 proposed multiplier which incorporates Wallace's technique and resulted in reduction of deepness of the circuit within creased speed and improved quantum cost, garbage outputs, and other parameters in nano-metric scales.

Saligram, R.[13] and Rakshith,T.[13] in 2013 proposed different Ancient mathematics technique to design a 4 bit parity conserving multiplier with less power consumption with the aid of The Total Reversible Logic Implementation Cost (TRLIC) for evaluation. This multiplier can be effectively used in FFTs filter and also in image processing applications.

M. Noorallahzadeh,[14] and M. Mosleh[14] suggested the importance of latches and designed eight new reversible blocks and also proposed novel designs of D, T, and J-K latches using reversible logic with improved quantum cost. Jais, A.[15], Palsodkar [15] proposed a very eventual 64 bit ancient multiplier which enhances the performance of DSP processors and shortens the complexity, consumption of power, area and delay. Results obtained are found with 33% reduction in delay.

Biswas, A.K., Hasan, M.M., Chowdhury, A.R.[6], HasanBabu, H.M.[7] proposed an effective reversible logic Utilizations of Binary Coded Decimal (BCD) adder and Bypass carry BCD adder with minimum number of gates and improved quantum cost.

III. REVERSIBLE LOGIC GATES

A. Not Gate

A NOT gate is 1x1 reversible gate. Conventional NOT gate is

reversible as demonstrated in Fig 1. When X1 is 0, the output will be 1 and when X1 is 1, it produces output as 0. The NOT gate holds the quantum cost of 1.

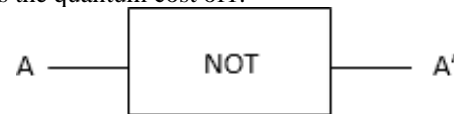


Fig.1 NOT gate

B. Feynman Gate

It is a 2x2 reversible gate. This gate holds the low quantum cost of 1. Gate in the Fig 2 performs inverse and XOR operation. It copies the value of A When B is 0 and inverses the value of A when B is 1. It also does the XOR operation with A and B.

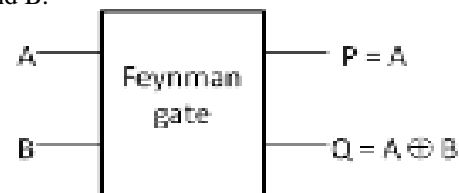


Fig. 2 Feynman gate

C. Peres Gate

It is a 3x3 reversible gate. Quantum cost of the gate is 4. Gate in the Fig 3 performs functions such as NOT, AND, NAND and XOR. It performs the operation of Half Adder. The output Q gives the value of Sum and output R gives the value of Carry. When B is 0, XOR operation of A and C will take place and when C is 0, AND operation of A and B will be done. The secondary output of this gate results in XOR operation with A and B.

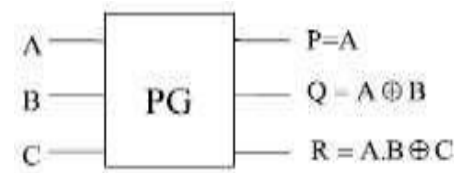


Fig. 3 Peres gate

D. DF Gate

It is a 3x3 reversible gate. It is called Double Feynman gate. The gate in the Fig.4 performs XOR operations for two different functions. One of the outputs is XOR of A and B. Another output is the XOR of A and C. P copies the value of A. Its quantum cost is 2 which is double that of Feynman gate. Hence, it is said to be Double Feynman gate.



Fig. 4 DFG gate

E. Toffoli Gate

It is a 3x3 reversible gate as demonstrated in fig. 5. Quantum cost is 5. When A is 0, it performs XOR operation of B and C. When B is 0, it does XOR operation of A and C. When C is 0, it does the AND operation with A and B. Hence Toffoli gate performs XOR and AND operation. When A=B=0, it act as copying gate of all three inputs. But it is mainly used for copying two inputs and for performing AND operation as XOR operation is generally performed with feynman gates.

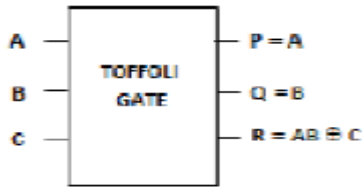


Fig.5 Toffoli gate

F. ZC Gate

It is a 4x4 reversible gate as demonstrated in Fig 6. This gate's quantum cost is 6. By assigning last two inputs as "0", it can implement the function of parity conserving reversible half-adder. The hardware complexity of this gate is same to $5\alpha + 2\beta + 1\gamma$.

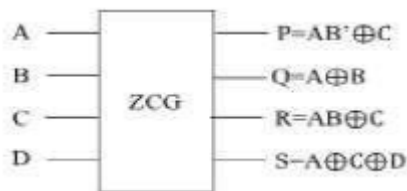


Fig. 6 ZC gate

G. HNG GATE

It is a 4x4 reversible gate as revealed in Fig 7. HNG is called Hybrid New Gate. All Boolean functions can be implemented using this gate. It performs operations such as AND, OR and XOR. HNG gate does the operation of Full Adder when 0 is assigned to D. R is Sum bit and S is Carry bit. HNG gate holds the quantum cost of 6.

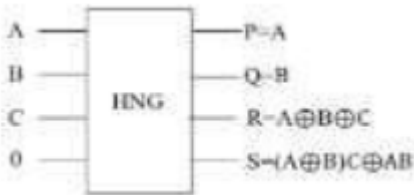


Fig. 7 HNG gate

H. Fredkin Gate

E. This gate is a 3x3 reversible gate as demonstrated in Fig 8 and may be a controlled swap gate. Quantum cost is 5 and has the hardware complexity same to $2\alpha + 4\beta + 1\gamma$ thanks to the very fact that there exist 2 unique XOR operations, 4 unique AND operations, and only 1 NOT operation in its output. This gate is considered as a universal gate. And it acts as buffer when the first input is 0.

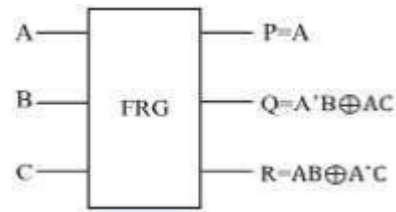


Fig. 8 FRG gate

I. ZPL Gate

ZPL is 5x5 parity-conserving reversible gate as established in Fig.9. Quantum cost is eight and its hardware complexity is same to $8\alpha + 3\beta + 1\gamma$. Almost like DFG, this gate acts as a parity-conserving full adder when last two inputs are assigned as zero. During this case, the output sum and carry are produced. Also, this gate produces the complete adder with minimum quantum cost.

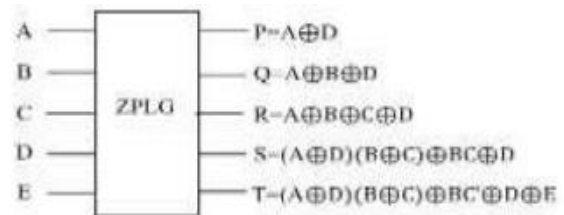


Fig. 9 ZPL gate

J. TV Gate

It is a 4x4 reversible gate. The gate in the Fig.10 performs XOR operation. Q gives the XOR of B and C. R gives the XOR of A and C. S is the sum bit of A, C and D where its carry bit is handled separately. P copied the value of A. Its quantum cost is 3. This gate is used as comparator circuit.

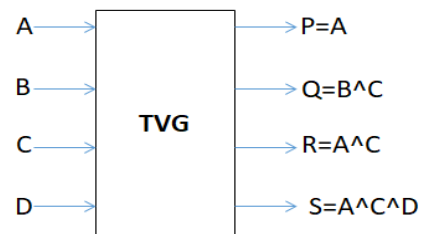


Fig. 10 TV gate

IV. ANCIENT METHODOLOGY

A. NikhilamSutra

This is the simplest way and specific method that provide shortcuts to multiply numbers that are closer to the power of 10 i.e 99&94, 998 & 986, 101 & 115.

B. AnurupyenaSutra

This is a sub-type of Nikhilam Sutra and functions on the concept of Working Base and then applies Nikhilam Sutra. It multiplies numbers that are not adjacent to power of 10 but are nearest to themselves.

C. Antyaordaske'pi

This multiplication sutra is applied where last digits of both numbers totals to 10.

D. Urdhva-Tiryakbhyam

The word "Urdhva-Tiryakbhyam" means upright and diagonal multiplication. This multiplication concept can be applied to all N bit numbers. This sutra is used for the multiplication of two numbers in decimal number system and binary number system. This type of multiplier has an advantage that the number of bits is directly proportional to area and delay and it raises gradually when correlated with other conventional multiplier.

E. Vinculum Process

Vinculum is a special method which is used with UrdhvaTiryak and this process is applied when numbers have bigger digits like 9,8,7,6 and is converted to smaller digits like 1,2,3,4 using Vinculum Process

F. EkanyunenaPurvena

It means one less than convius one and is applicable for multiplication of two numbers where multiplicand is any number and multiplier is 9 or array of 9.

V. PROPOSED REVERSIBLE ANCIENT MULTIPLIER

This proposed system of ancient multiplier eliminates unwanted multiplication steps. The proposed technique will be accustomed to propagate any variety of numbers. The designed work requires only few processes with better hardware complexity. The result is assembled in one place with limited memory consumption.

A. Proposed 4- Bit Ancient Multiplier

A standard block diagram of a 4-bit Ancient multiplier requires three levels, during which four 2-bit Ancient multipliers are employed in the primary level, two 4-bit ripple carry summers within the secondary level, and one 4-bit ripple carry summer within the tertiary level.

B. 4x4 Bit Ancient Multiplier

As demonstrated in Fig.13, a custom design of a 4-bit Ancient multiplier requires three levels, during which four 2-bit Ancient multipliers are utilized in the primary level, two 4-bit ripple carry summers within the second level, and one 4-bit ripple carry summer within the third level. In the following, two proposed 4-bit reversible Ancient multipliers are described. To implement the reversible Ancient multiplier provided in Fig.12, it's necessary to implement all the used modules in it with reversible circuits. Proposed 2-bit Ancient multiplier module is demonstrated in Fig.11.

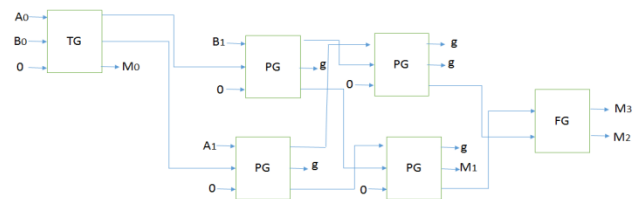


Fig. 11 Reversible 2-bit Ancient Multiplier

This circuit requires 1 tofolli gate and five Peres gates. The amount of its constant input and its garbage outputs is same to 5. Quantum cost is22.

Also, Utilization of a reversible 4-bit ripple carry summer using the HNG block and Peres gate is demonstrated in Fig. 12. A and B are 2-bit inputs. S is 4-bit output and C0 is the Carry output. Therefore, the 4-bit reversible ripple carry summer has constant input number same to 4, the garbage output is 7 and the quantum cost is22.

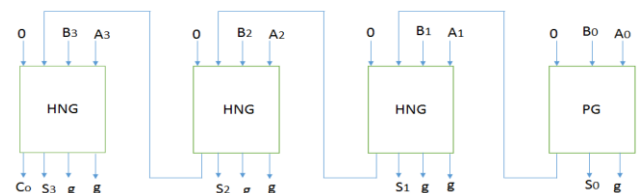


Fig. 12 Reversible 4-bit Ripple carry summer.

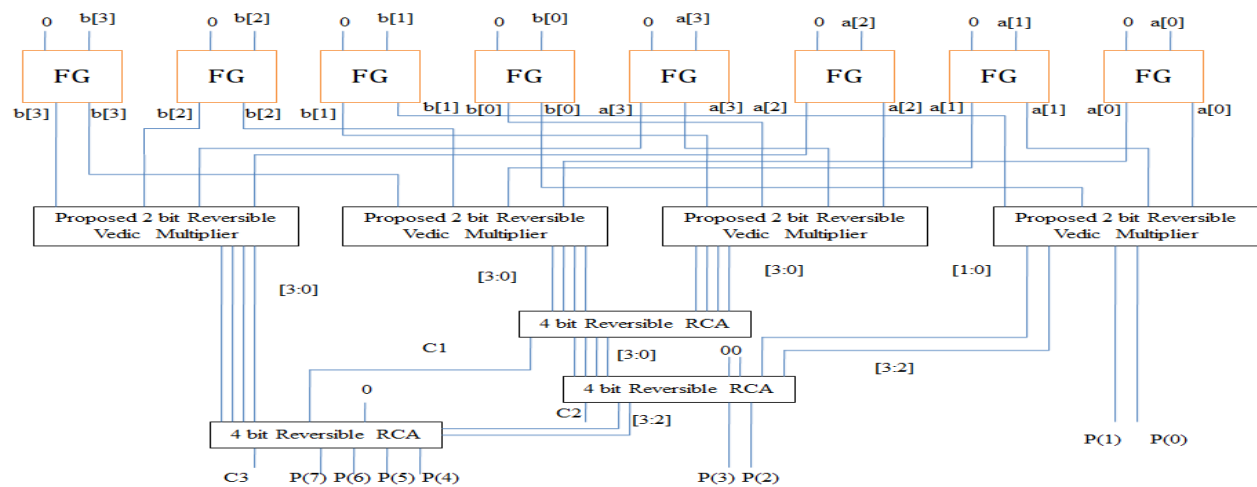


Fig. 13 4x4 Bit Reversible Ancient multiplier

The 4-bit Ancient multiplier contains 8 Feynman gates, 4 2-bit Ancient multiplier and 3 4-bit ripple carry summer. Where a and b are 4-bit inputs. P is 8-bit output. The quantum cost for the 4-bit Ancient multiplier is 162. Proposed 4-bit reversible Ancient multiplier block diagram is demonstrated in Fig.13.

The proposed circuit includes 1 PPTG, 3 Fredkin gates and 2 ZCG as demonstrated in fig.14, all of which are capable of parity conserving. The number of constant inputs as well as garbage outputs is same to 8. In addition, the quantum cost is 30.

B. 4x4 Bit Parity Conserving Ancient Multiplier

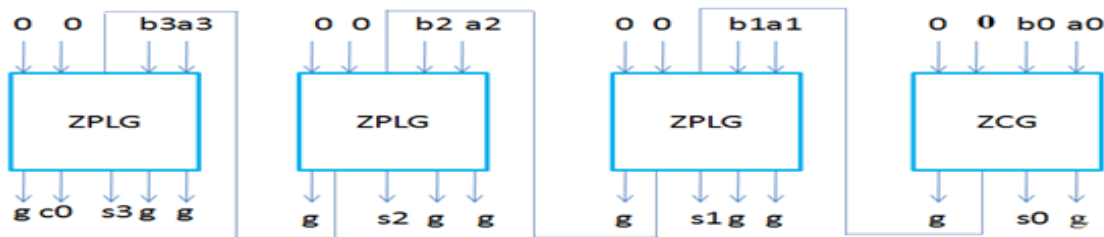


Fig. 14 2*2 Reversible Ancient Multiplier with Parity Conserving

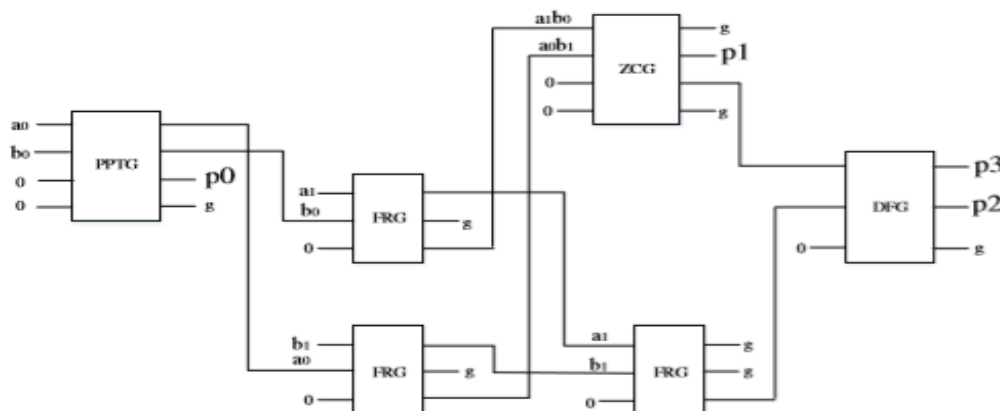


Fig. 15 4x4 Parity Conserving Reversible Ripple carry summer

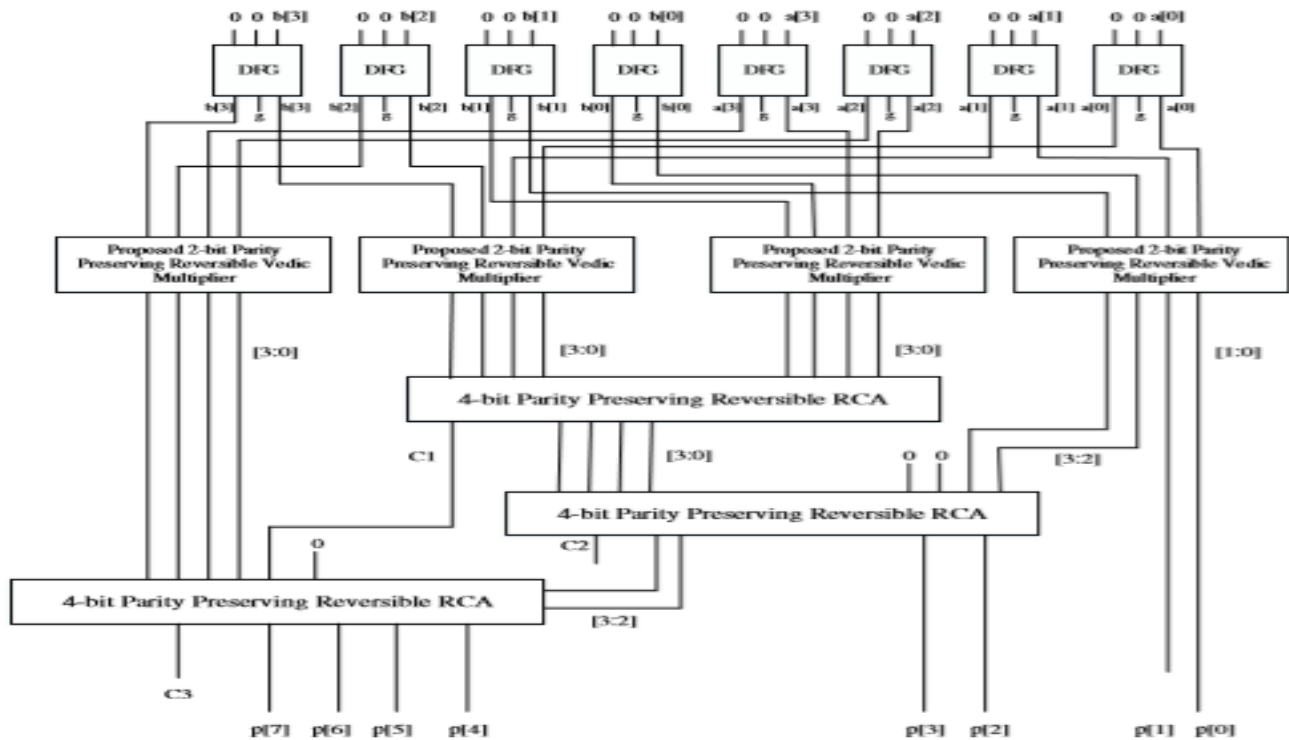


Fig. 16 4*4 Reversible Ancient Multiplier with Parity Conserving

From fig.15, the obtained constant inputs and garbage outputs of the 4-bit Parity Conserving reversible ripple carry summer are 8 and 11, respectively. It holds the quantum cost is $[(3 \times 8) + 6] = 30$. Proposed 4-bit reversible Ancient multiplier with parity conserving block diagram is demonstrated in fig.16. Therefore, the obtained quantum cost of the design is 226.

C. Proposed 8 Bit Ancient Multiplier

A custom design of a 8-bit Ancient multiplier is consists of three levels, in which four 4-bit Ancient multipliers have been used in the first level, two 8-bit ripple carry summers in the

second level, and one 8-bit ripple carry summer in the third level.

D. 8x8 Reversible Ancient Multiplier

Utilization of a reversible 8-bit ripple carry summer using the HNG and Peres gate is demonstrated in Fig. 17. A and B are 4-bit inputs. S is 8-bit output and C0 is the Carry output. Therefore, the 4-bit reversible ripple carry summer has constant input number same to 8, the garbage output of 15 and the quantum cost of 46.

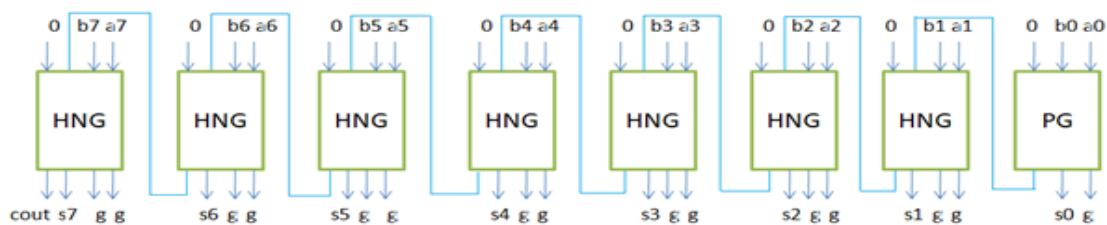


Fig. 17 8*8 Reversible Ancient multiplier ripple carry summer

The 8-bit Ancient multiplier comprises of sixteen Feynman gates, four 4-bit Ancient multiplier and three 8-bit ripple carry summer. a and b are 8-bit inputs. P is 16-bit output. The quantum cost of 4-bit Ancient multiplier is 162. Proposed 8-bit reversible Ancient multiplier is demonstrated in fig. 18. Therefore, the quantum cost of the proposed reversible Ancient multiplier is calculated as 802.

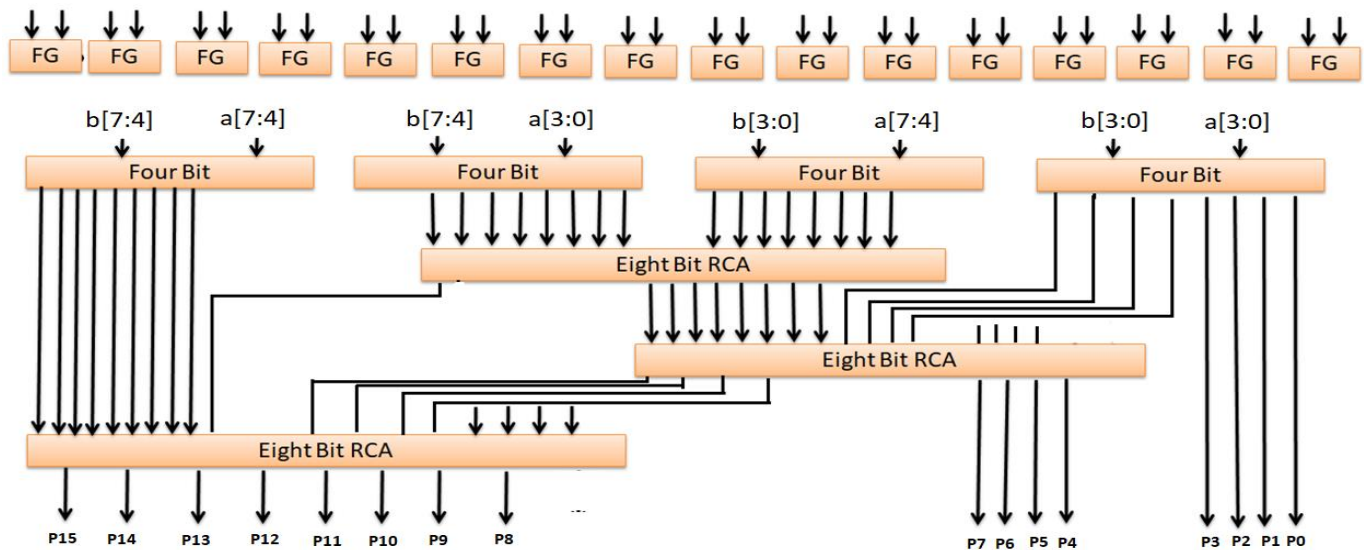


Fig. 18 8x8 Reversible Ancient Multiplier

E. 8x8 Bit Parity Conserving Ancient Multiplier

Utilization of a reversible 8-bit ripple carry summer using the ZPL and ZCG gate is demonstrated in fig.19. A and B are 16-bit inputs. S is 8-bit output and C0 is the Carry output.

Therefore, the 8-bit reversible ripple carry summer has constant input number same to 16, the garbage output of 15 and the quantum cost of 62.

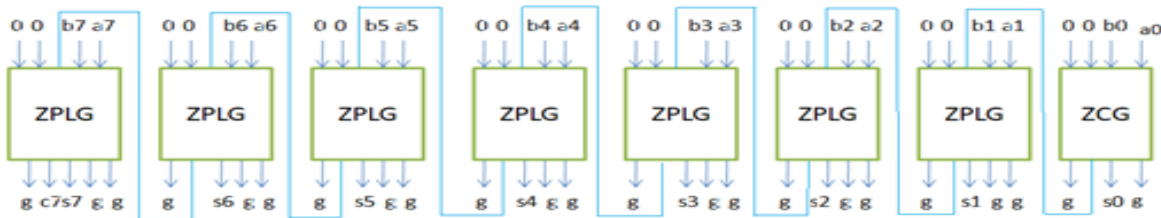


Fig. 19 8x8 Parity conserving reversible ripple carry summer

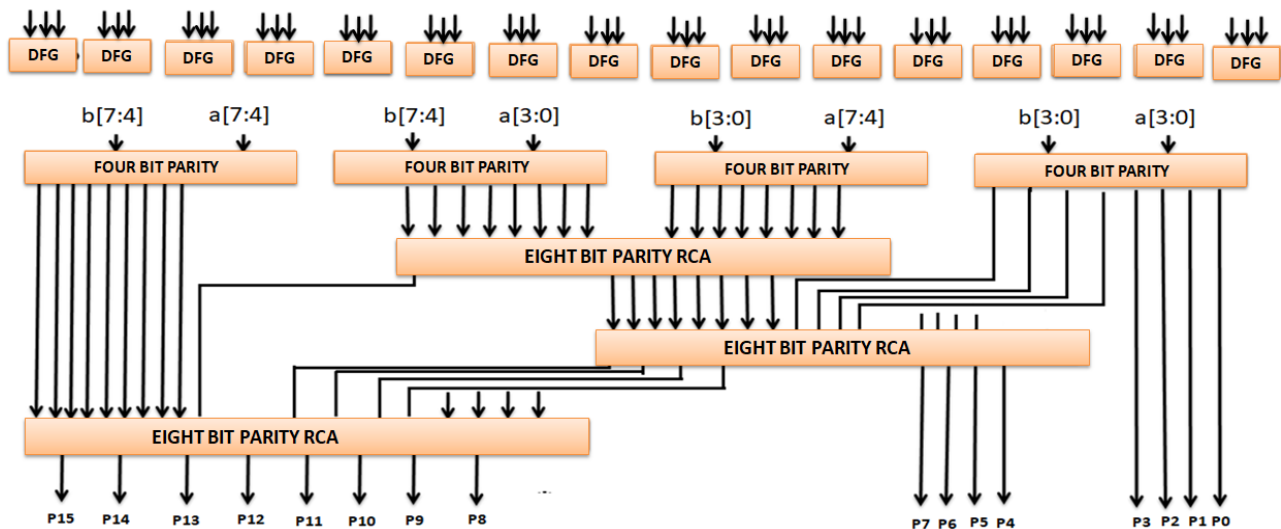


Fig. 20 8x8 Reversible Ancient Multiplier with Parity Conserving

The 8-bit parity conserving Ancient multiplier comprises of 16 double Feynman gates, four 4-bit Ancient multiplier and three 8-bit ripple carry summer. A and B are 16-bit inputs. P is 8-bit output. Proposed 16-bit reversible Ancient multiplier is demonstrated in Fig.20. Therefore, the quantum cost of the proposed reversible Ancient multiplier is calculated as 1122.

F. Proposed 16 Bit Ancient Multiplier

A standard design of a 16-bit Ancient multiplier is consists of three levels, in which four 8-bit Ancient multipliers have been used in the first level, two 16-bit ripple carry summers in the

second level, and one 16-bit ripple carry summer in the third level.

G. 16x16 Reversible Ancient Multiplier

Utilization of a reversible 16-bit ripple carry summer using the HNG and Peres gate is demonstrated in Fig.21. A and B are 16-bit inputs. S is 16-bit output and C0 is the Carry output. Therefore, the 16-bit reversible ripple carry summer has obtained constant input same to 16, the garbage output of 31 and the quantum cost of 94.

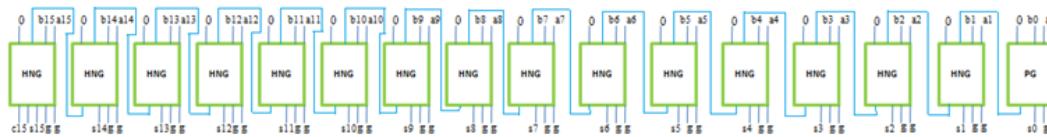


Fig. 21 Reversible 16-bit Ripple carry summer

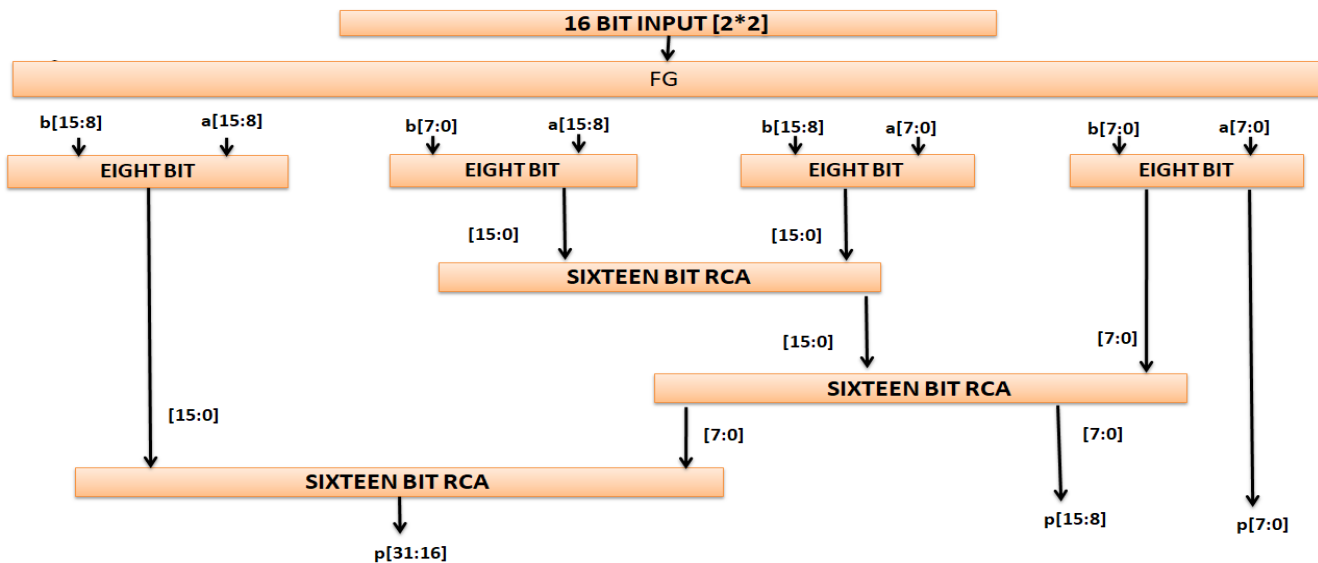


Fig. 22 16x16 Bit Reversible Ancient multiplier

The 16-bit Ancient multiplier comprises of 32 Feynman gates, four 8-bit Ancient multiplier and three 16-bit ripples carry summer as demonstrated in fig.22. A and B are 16-bit inputs. P is 32-bit output. The quantum cost of 16-bit Ancient multiplier is 3522.

H. 16x16 Bit Parity Conserving Ancient Multiplier

Utilization of a reversible 16-bit ripple carry summer using the ZPL block and ZCG gate is demonstrated in Fig.

23. A and B are 32-bit inputs. S is 16-bit output and C0 is the Carry output. Therefore, the 16-bit reversible ripple carry summer holds constant input number 32, the garbage output of 47 and the quantum cost of 111.

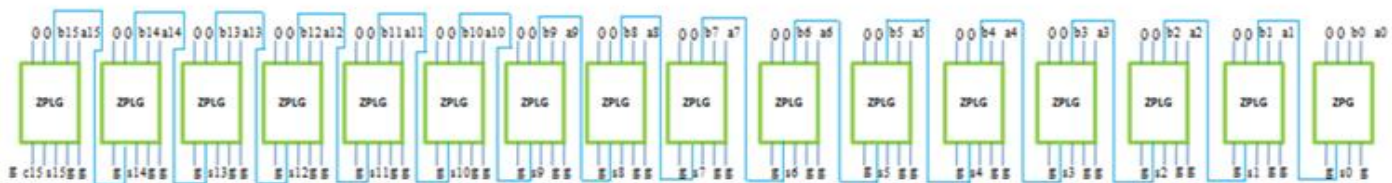


Fig. 23 16x16 Parity Conserving Reversible Ripple carry summer

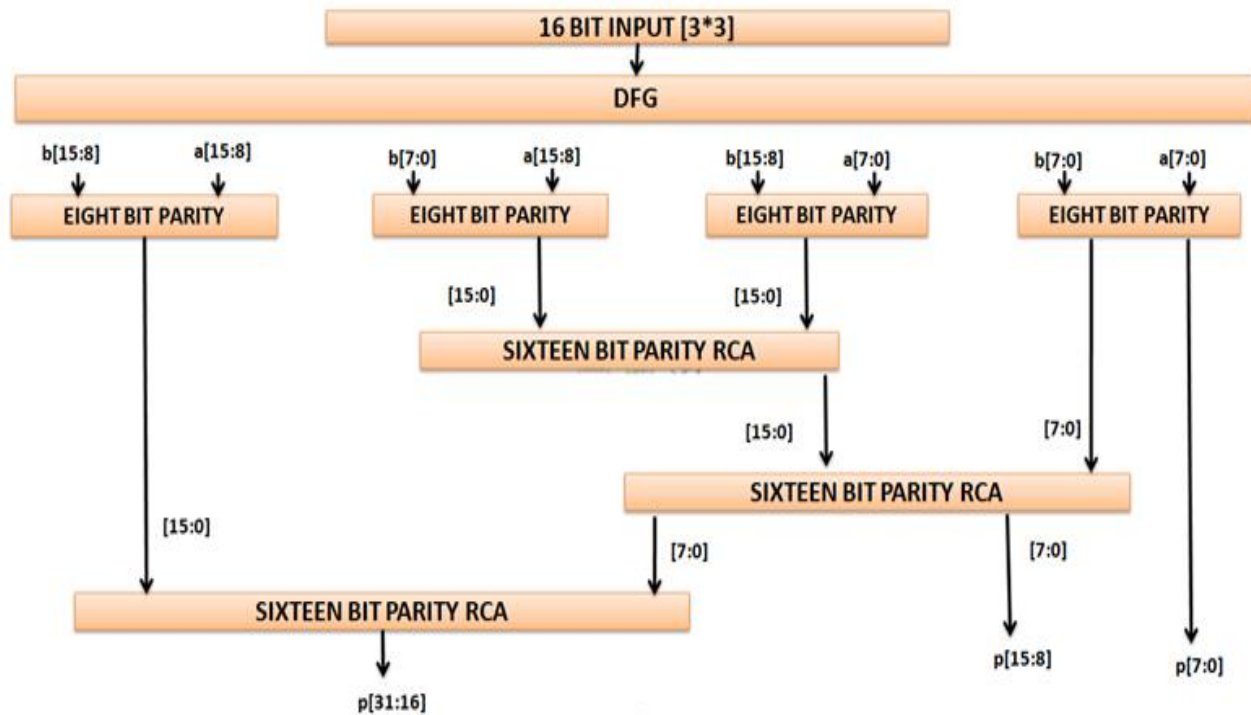


Fig. 24 16x16 Reversible Ancient Multiplier with Parity Conserving

The 16-bit parity conserving Ancient multiplier comprises of 32 Double Feynman gates, four 8-bit Ancient multiplier and three 16-bit ripple carry summer. A and B are 16-bit inputs. P is 32-bit output. Proposed 16-bit reversible Ancient multiplier with parity conserving is demonstrated in fig.24. Therefore, the quantum cost of the design is calculated as 4930.

I. Proposed 32 Bit Ancient Multiplier

A standard design of a 32-bit Ancient multiplier is consists of three levels, which consists four 16-bit Ancient multipliers in

the first level, two 32-bit ripple carry summers in the second level, and one 32-bit ripple carry summer in the third level.

J. 32x32 Reversible Ancient Multiplier

Utilization of a reversible 32-bit ripple carry summer using the HN gate and Peres gate is demonstrated in fig.25. A and B are 32-bit inputs. S is 32-bit output and C0 is the Carry output. Therefore, the 32-bit reversible ripple carry summer has obtained 32 constant input, the garbage output of 63 and the quantum cost of 190.

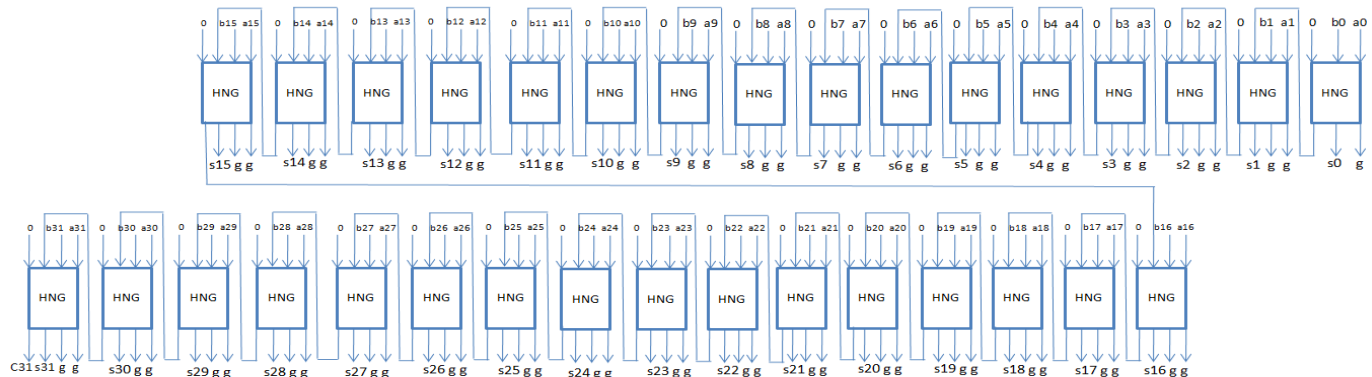


Fig. 25 Reversible 32-bit Ripple carry summer

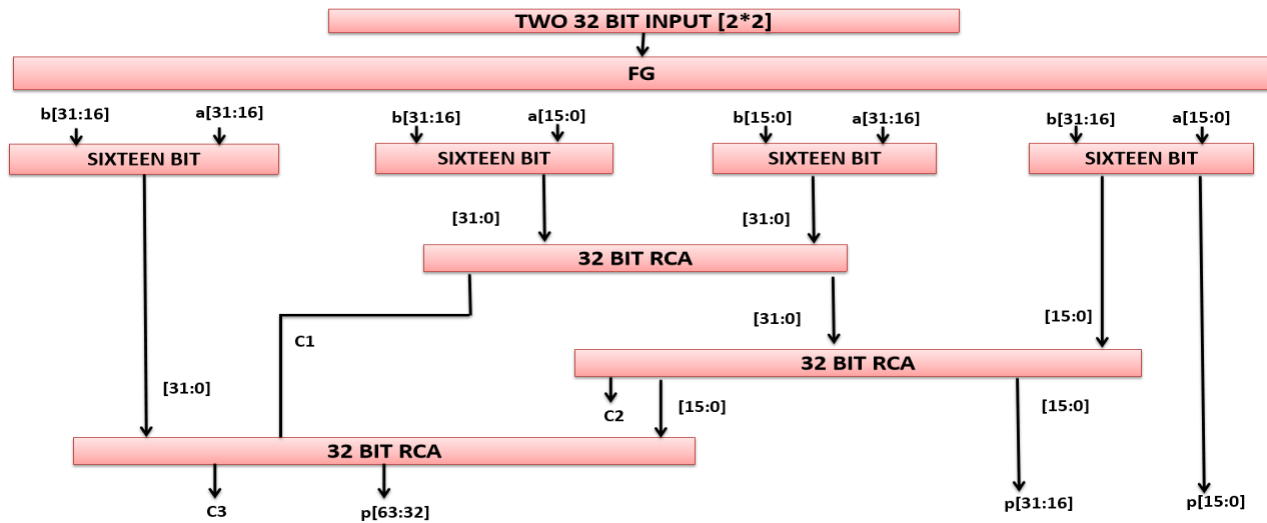


Fig. 26 32x32 Bit Reversible Ancient multiplier

The 32-bit Ancient multiplier comprises of 64 Feynman gates, four 16-bit Ancient multiplier and three 32-bit ripple carry summer. A and B are 32-bit inputs. P is 64-bit output. The obtained quantum cost of 32-bit Ancient multiplier is 14722.

the ZPL block and ZCG gate is demonstrated in fig.27. A and B are 64-bit inputs. S is 32-bit output and C is the Carry output. Therefore, the 32-bit reversible ripple carry summer has constant input number same to 64, the garbage output of 95 and the quantum cost of 254

K. 32x32 Bit Parity Conserving Ancient Multiplier

Utilization of a reversible 32-bit Ripple Carry Summer using



Fig. 27 32x32 Parity Conserving Reversible Ripple carry summer

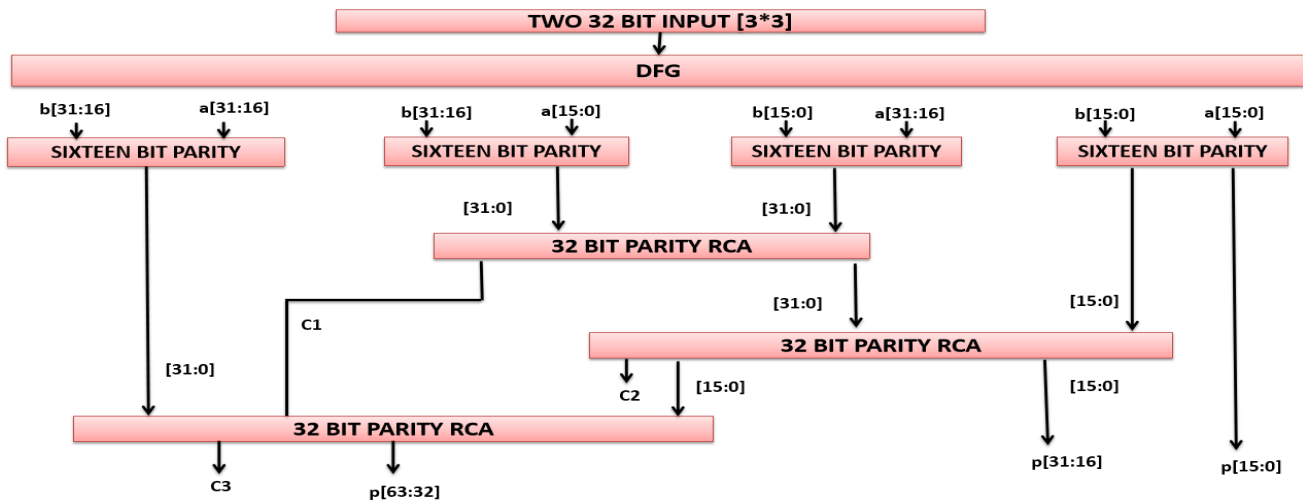


Fig. 28 32x32 Reversible Ancient Multiplier with Parity Conserving

The 32-bit Ancient multiplier with parity conserving comprises of four 16-bit Ancient multiplier, 64 Double Feynman gates, and three 32-bit ripple carry summer. A and B are 32-bit inputs. P is 64-bit output. Proposed 32-bit reversible Ancient multiplier with parity conserving is demonstrated in fig.28. Therefore, the obtained quantum cost of the design is 20610.

VI. RESULT AND DISCUSSION

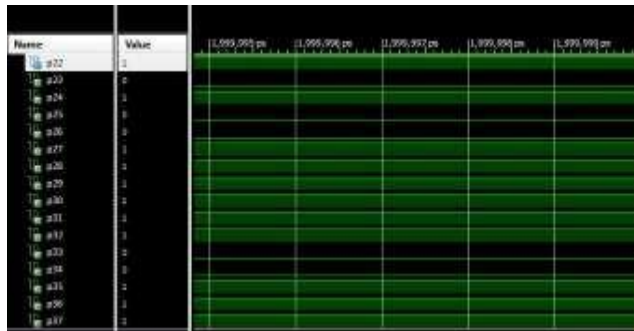


Fig. 29 Simulation results for 32x32 Reversible Ancient Multiplier

In a 32x32 reversible Ancient multiplier when a two 32-bit input such as $a=10011010110010100001110001111010$ and $b=00010111010111010110011000011110$ is given, it gets multiplied using urdhvatiryak sutra which enables parallel generation of multiplication and addition and the output will be obtained in 64 bits $p=01110001000001010000110111001111100101011001111$

Table 1 ASIC parameter results

	4 bit vedic multiplier		8 bit vedic multiplier		16 bit vedic multiplier		32 bit vedic multiplier	
	Without Parity	With Parity	Without Parity	With Parity	Without Parity	With Parity	Without Parity	With parity
Leakage power	2415.474	2081.443	12851.602	10382.166	57599.448	45690.051	243268.084	191016.218
Dynamic power	13666.53	9183.005	101067.39	59475.556	591562.83	324112.30	3159842.03	1701634.48
Total power(nW)	16081.526	11264.448	113918.99	69857.732	649162.284	369802.35	3403110.12	1892650.70
Area (nm ²)	356	345	1902	1743	8542	7762	36105	32661
Delay (ps)	2578	2224	6078	4418	11902	8440	23066	16024
Gate count	56	36	304	176	1376	760	5840	3144

001010000000.

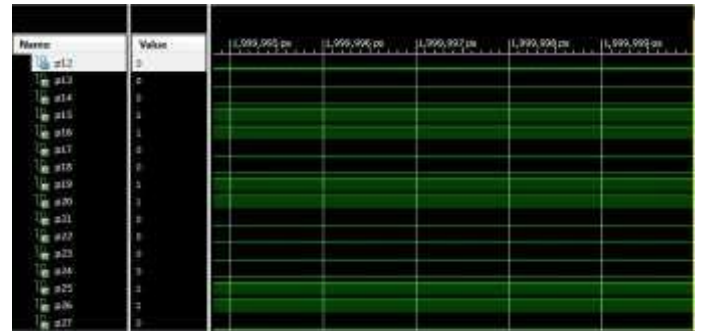


Fig. 30 Simulation results for 32x32 Reversible Ancient Multiplier with Parity Conserving

In a 32x32 reversible Ancient multiplier with parity conserving, when a two 32-bit input such as $a=11001101100110111100101000110011$ and $b=00001110101110001111100101000011$ is given, it gets multiplied using urdhva tiryak sutra which enables parallel generation of multiplication and addition and the output will be obtained in 64 bits $p=010111101001100010101001110100111011000011001100011010000000$. The simulation results implemented on Xilinx Spartan 6E is demonstrated in fig.29 and fig.30. The below are the performance results obtained from implementing the code in 90nm technology of CADENCE EDA tool.

Table 2 Quantum Parameter Results

	4 bit vedic multiplier		8 bit vedic multiplier		16 bit vedic multiplier		32 bit vedic multiplier	
	Without Parity	With Parity	Without Parity	With Parity	Without Parity	With Parity	Without Parity	With Parity
Quantum Cost	162	226	802	1122	3522	4930	14722	20610
Constant Input	43	76	212	384	928	1696	3812	7104
Garbage Output	44	73	224	348	992	1496	4012	6975

VI. COMPARISON AND EVALUATION RESULTS

The 4-bit reversible Ancient multiplier with parity conserving technique is 29.9% more effective than 4-bit reversible Ancient multiplier without parity with respect to total consumption of power and 3% more effective with respect to area consumption and 13% more effective with respect to delay. The 8-bit reversible Ancient multiplier with parity conserving technique is 38% more effective than 8-bit reversible Ancient multiplier without parity with respect to total consumption of power and 8.3% more effective with respect to area consumption and 27.3% more effective with respect to delay. The 16-bit reversible Ancient multiplier with parity conserving technique is 43% more effective than 16-bit reversible Ancient multiplier without parity with respect to total consumption of power and 9.1% more effective with respect to area consumption and 29% more effective with respect to delay. 32-bit reversible Ancient multiplier with parity conserving technique is 44.3% more effective than 32-bit reversible Ancient multiplier without parity with respect to total consumption of power and 9.5% more effective with respect to area consumption and 30.5% more effective with respect to delay.

VII. CONCLUSION

The proposed reversible Ancient multiplier consists of two effective 4, 8, 16 and 32 bit Ancient multipliers using reversible logic gates. The comparison results have demonstrated that the proposed reversible multipliers are more efficient with respect to quantum parameters correlated with other existent designs. The reversible Ancient multiplier with parity conserving technique is more effective than the reversible Ancient multiplier without parity conserving technique with respect to ASIC parameters.

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