International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9 Issue-5, March 2020

Three Level Inverter Controlled UPFC for Harmonic Reduction using Space Vector Pulse Width Modulation Technique

R. Jayachandra, G. Tulasi Ram Das

Abstract: ***Unified Power Flow Controller (UPFC) is one of the most important device in FACTS family, this device in this work is used for power quality improvement. In this paper three level inverter is proposed for UPFC for the reduction of harmonics and for the enhancement of power transfer capability. SVPWM technique decides switching pattern of three level inverter. Therefore, in this paper this method is applied for controlling the three level inverter output. The proposed method is applied on four bus system and results are compared with UPFC without three level inverter. Results demonstrated that the proposed method effectively decreasing the harmonics and increasing the power transfer capability.***

Index Terms: Multilevel Inverter (MLI); Unified Power Flow Controller(UPFC); Space Vector Pulse Width Modulation (SVPWM).

I. INTRODUCTION

Now a day's power quality is the major problem in an interconnected power system. In an interconnected power system the power transfer through transmission lines can be increased by using FACTS devices without violating the limits. UPFC is one of the versatile device in facts family. UPFC can be operated independently and simultaneously for controlling the power flow effecting parameters like impedance, voltage and phase angle. This device not only used for power transfer, it can be used for angle stability and also voltage stability. Voltage stability involves maintaining the voltage within the acceptable limits and harmonics elimination. Conventional UPFC consist of two transformers, two voltage source inverters and dc link capacitor. In conventional UPFC harmonics are more because of voltage source inverter [1-3].On the other hand multilevel inverters are used for reducing harmonics.

Different types of multilevel inverters are Diode clamped, flying capacitor and cascaded. Because of number of advantages with Cascade Multilevel inverters over other, In most of the applications cascaded Multilevel inverters (CMLI) were used [4-7]. The performance of CMLI depends on pulse generation pattern. Different types of Pulse width modulation (PWM) techniques have been developed for reducing the total harmonic content. SVPWM technique is considered as a best method of generating pulses for Cascaded multilevel inverter because of better fundamental output voltage, reduced THD and easy to implement[8-11].

In this paper space vector pulse width modulation technique is used for generation of pulses to Unified power flow controller voltage source inverter.

Revised Manuscript Received on March 30, 2020.
* Correspondence Author
R Jayachandra*, Research Scholar, EEE Dept, JNTUH, Hyderabad, saimedha.J@gmail.com
Dr G Tulasi Ram Das, Professor, EEE Department, JNTUH, Hyderabad, das123tulasiram@gmail.com.

II. IMPLEMENTATION OF ROPOSED METHOD

Space vector pulse width modulation technique implementation involves three stages [12-15]:

Stage 1: calculation of Vd , Vq and angle α

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \left(\frac{2}{3}\right)\begin{bmatrix} 1 & \frac{-1}{2} & \frac{-1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} \quad (1)$$

$$\left|V_{ref}\right| = \sqrt{V_d^2 + V_q^2} \quad (2)$$

$$\alpha = \tan^{-1}\left(\frac{V_q}{V_d}\right) \quad (3)$$

Where V_{an}= phase A voltage
V_{bn}=phase B voltage
V_{cn}=phase C Voltage

V_d, V_q, V_{ref} and α are calculated by using equations 1 to 3.

Stage 2: Time duration calculation ($T1, T2, T0$)

$$T_z\left|V_{ref}\begin{bmatrix}\cos(\alpha)\\ \sin(\alpha)\end{bmatrix}\right| = T_1\frac{2}{3}V_{dc}\begin{bmatrix}1\\0\end{bmatrix} + T_2\frac{2}{3}V_{dc}\begin{bmatrix}\cos\left(\frac{\pi}{3}\right)\\ \sin\left(\frac{\pi}{3}\right)\end{bmatrix}$$

$$T_1 = T_Z * a * \frac{\sin\left(\frac{\pi}{3}-\alpha\right)}{\sin\left(\frac{\pi}{3}\right)} \quad (4)$$

$$T_2 = T_Z * a * \frac{\sin(\alpha)}{\sin\left(\frac{\pi}{3}\right)} \quad (5)$$

$$T_0 = T_Z - (T_1 + T_2) \quad (6)$$

Where $T_Z = \frac{1}{f}$

$$a = \frac{|V_{ref}|}{\frac{2}{3}V_{dc}}$$

For sector 1 switching time durations are calculated using the equations 4 to 6.

$$T_1 = \frac{\sqrt{3} * T_Z * |V_{ref}|}{V_{dc}} * \left(\sin\frac{n*\pi}{3} * \cos(\alpha) - \cos\frac{n*\pi}{3} * \sin(\alpha)\right) \quad (7)$$

$$T_2 = \frac{\sqrt{3} * T_Z * |V_{ref}|}{V_{dc}} * \left(-\sin\frac{n-1}{3} * \cos(\alpha) + \cos\frac{n-1}{3} * \sin(\alpha)\right) \quad (8)$$

$$T_0 = T_Z - (T_1 + T_2) \quad (9)$$

Where α= 0 to 60 degrees.

n= no of switching states (6 for three level)

For any sector switching times are calculated by using equations 7 to 9.

Stage 3: Calculation of switching time for switches (S1 to S6)

TABLE 1
SWITCHING TIME FOR SECTORS

Sector	S1,S3,S5	S4,S6,S2
I	$S_1 = T_1 + T_2 + \frac{T_0}{2}$ $S_3 = T_2 + \frac{T_0}{2}$ $S_5 = \frac{T_0}{2}$	$S_2 = T_1 + T_2 + \frac{T_0}{2}$ $S_6 = T_1 + \frac{T_0}{2}$ $S_4 = \frac{T_0}{2}$
II	$S_1 = T_1 + \frac{T_0}{2}$ $S_3 = T_1 + T_2 + \frac{T_0}{2}$ $S_5 = \frac{T_0}{2}$	$S_2 = T_1 + T_2 + \frac{T_0}{2}$ $S_6 = \frac{T_0}{2}$ $S_4 = T_2 + \frac{T_0}{2}$
III	$S_1 = \frac{T_0}{2}$ $S_3 = T_1 + T_2 + \frac{T_0}{2}$ $S_5 = T_2 + \frac{T_0}{2}$	$S_2 = T_1 + \frac{T_0}{2}$ $S_6 = \frac{T_0}{2}$ $S_4 = T_1 + T_2 + \frac{T_0}{2}$
IV	$S_1 = \frac{T_0}{2}$ $S_3 = T_1 + \frac{T_0}{2}$ $S_5 = T_1 + T_2 + \frac{T_0}{2}$	$S_2 = \frac{T_0}{2}$ $S_6 = T_2 + \frac{T_0}{2}$ $S_4 = T_1 + T_2 + \frac{T_0}{2}$
V	$S_1 = T_2 + \frac{T_0}{2}$ $S_3 = \frac{T_0}{2}$ $S_5 = T_1 + T_2 + \frac{T_0}{2}$	$S_2 = \frac{T_0}{2}$ $S_6 = T_1 + T_2 + \frac{T_0}{2}$ $S_4 = T_1 + \frac{T_0}{2}$
VI	$S_1 = T_1 + T_2 + \frac{T_0}{2}$ $S_3 = \frac{T_0}{2}$ $S_5 = T_1 + \frac{T_0}{2}$	$S_2 = T_2 + \frac{T_0}{2}$ $S_6 = T_1 + T_2 + \frac{T_0}{2}$ $S_4 = \frac{T_0}{2}$

III. TEST SYSTEM & RESULTS

Four Bus systems shown in fig.1 is taken for testing the effectiveness of the proposed method.

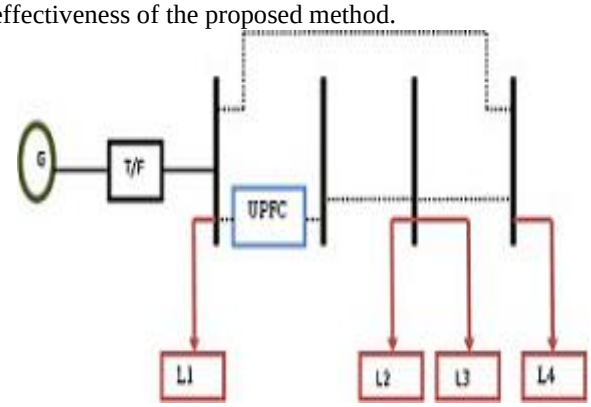

Fig.1 Test system

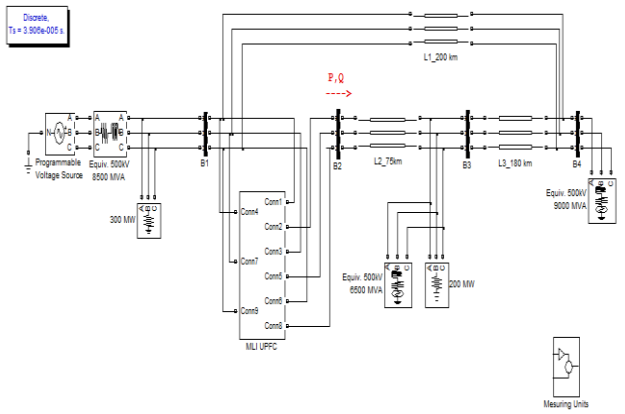

Fig.2 Simulation diagram of SVPWM three level UPFC

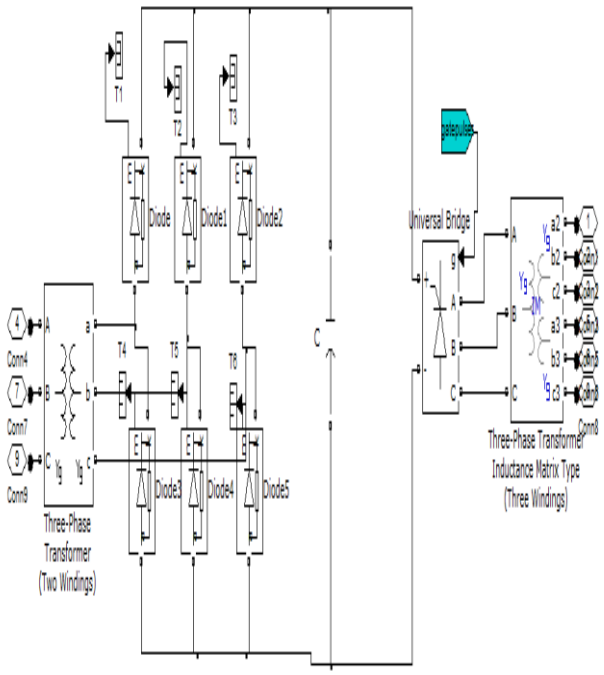

Fig.3 MLI based UPFC internal structure.

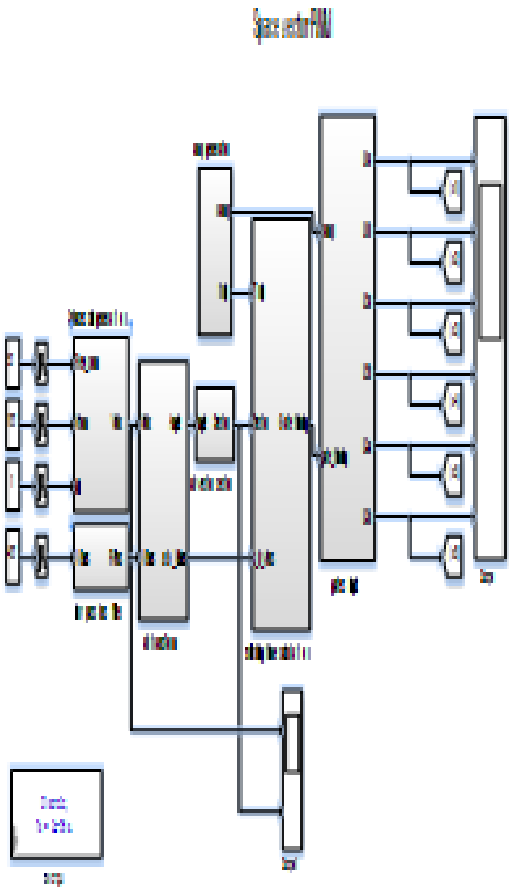

Fig.4 SVPWM Pulse Generation Pattern.

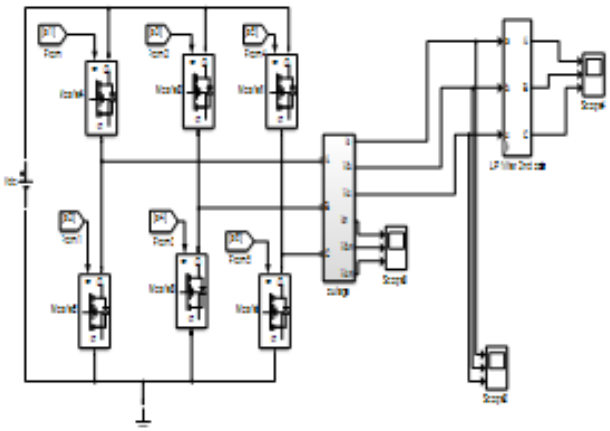

Fig.5 Three level inverter of UPFC.

Fig.5 shows pulse generating pattern of svpwm technique, these pulses are generated based on the equations 7 to 9 provided. The respective phase voltages of all phases are shown in fig.6 to fig.8. FFT analysis for line as well as phase voltages is shown in fig.9 and 10.

Fig.6 Pulse generations for switches S1-S6 with respect to time.

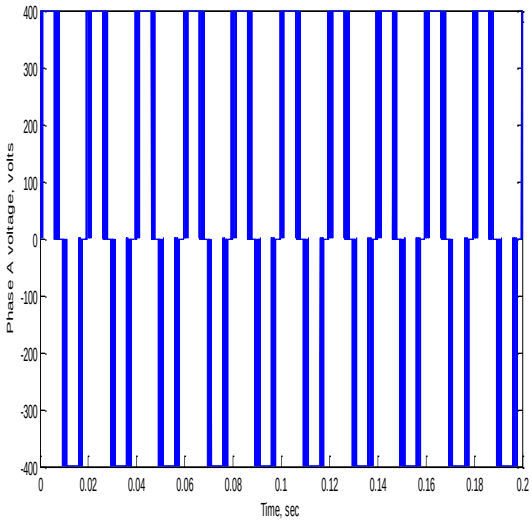

Fig.7 phase a voltage of three level inverter

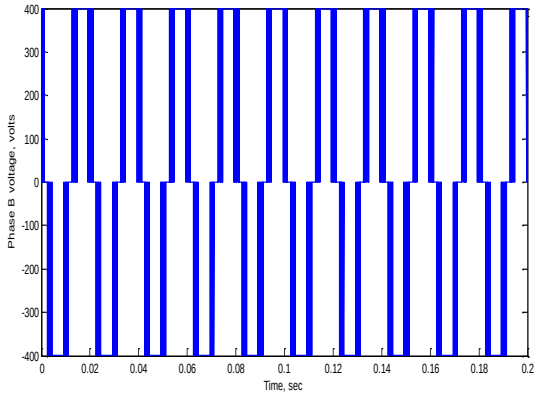

Fig.8 phase b voltage of three level inverter

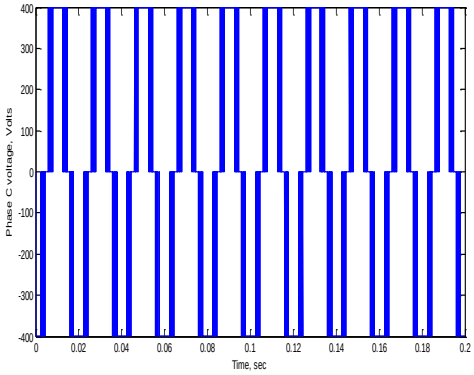

Fig.8 phase c voltage of three level inverter

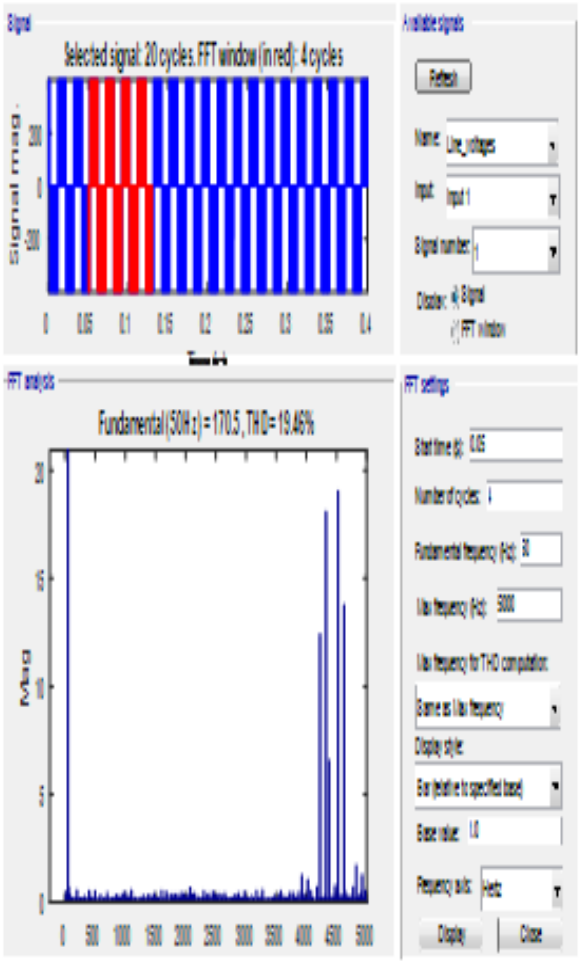

Fig.9 FFT analysis of phase voltage with three level inverter for UPFC

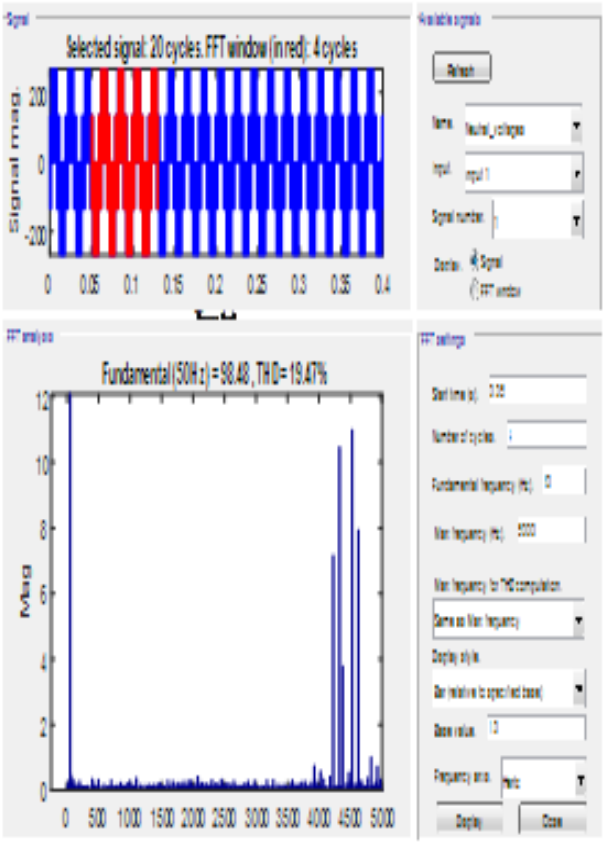

Fig.10 FFT analysis of Line voltage with three level inverter for UPFC

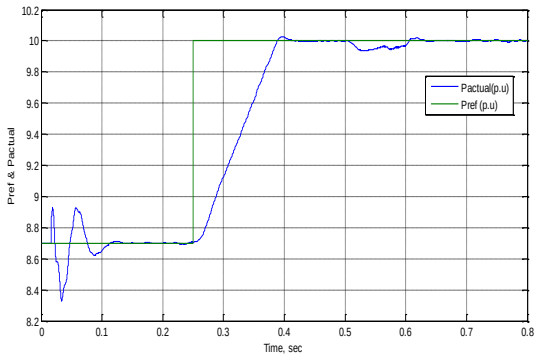

Fig.11 Real power with respect to time with three level inverter for UPFC

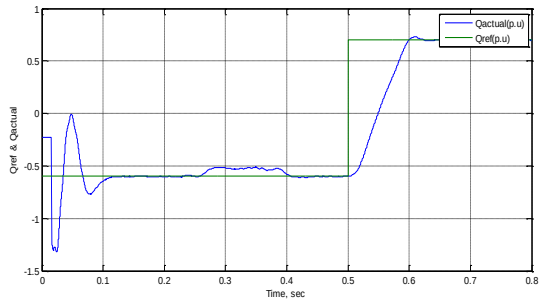

Fig.12 Reactive power with respect to time with three level inverter for UPFC

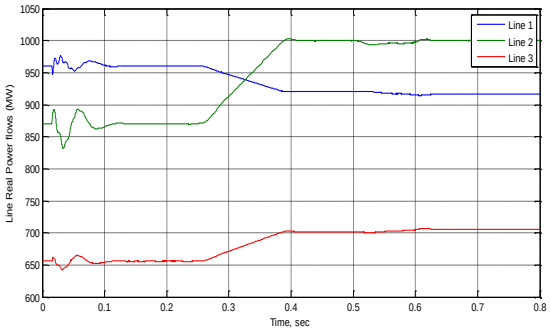

Fig.13 Real power in Lines with respect to time with three level inverter for UPFC

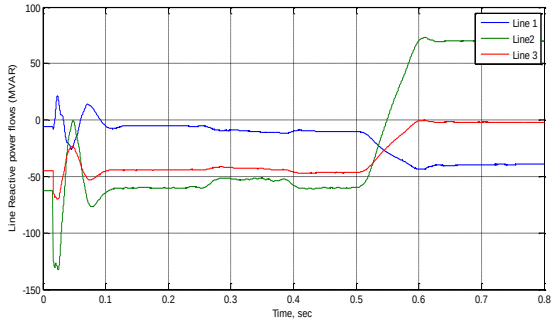

Fig.14 Reactive power in Lines with respect to time with three level inverter for UPFC

Table 2 indicates real and reactive power flow through line 1 with and without Three level inverter of UPFC.

TABLE 2
REAL & REACTIVE POWER FLOW WITH AND WITHOUT MLI

	P(MW)	Q(MVAR)	THD
UPFC Without MLI	970	60	60.19
UPFC With MLI	980	63.3	19.47

IV. CONCLUSIONS

The effectiveness of the proposed method is tested on four bus system, From figures 6 to 12 and table 2, we concluded that Three level inverter model of UPFC increases power flow and decreases total harmonic distortion in the power system. Therefore, svpwm based three level inverter of UPFC is better than without three level inverter.

REFERENCES

1. N.G Hingorani, "High Power Electronics and Flexible AC Transmission Systems", IEEE. Power Engineering Review, 1988
2. C. Schauder, "Development of a Â 100Mvar Static Condenser for Voltage control of Transmission systems", IEEE transactions on Power delivery, vol. 10, no. 3, pp. 1486-1496, 1995
3. E. Joncquel and X. Lombard, "A Unified Power flow Controller for the ElectroMagnetic Transients Program", 6th European Conf. Power Electronics and Applications, 1995
4. R. H. Baker and L. H. Bannister, "Electric Power Converter," U.S. Patent 3 867 643, Feb. 1975.

5. A. Nabae, I. Takahashi, and H. Akagi, “A New Neutral-point Clamped PWM inverter,” IEEE Trans. Ind. Applicat., vol. IA-17, pp. 518-523, Sept./Oct. 1981.
6. F. Z. Peng and J. S. Lai, “Multilevel Cascade Voltage-source Inverter with Separate DC source,” U.S. Patent 5 642 275, June 24, 1997.
7. N. S. Choi, J. G. Cho, and G. H. Cho, “A general circuit topology of multilevel inverter,” in Proc. IEEE PESC’91, 1991, pp. 96–103.
8. Active Harmonic Elimination for Multilevel Converters; Du, Z.; Tolbert, L.M.; Chiasson, J.N.; Power Electronics, IEEE Transactions on Volume 21, Issue 2, March 2006 Page(s):459 – 469.
9. Low switching frequency active harmonic elimination in multilevel converters with unequal DC voltages; Zhong Du; Tolbert, L.M.; Chiasson, J.N.; Hui Li; Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005, Volume 1, 2-6 Oct. 2005 Page(s):92 - 98 Vol. 1.173
10. Elimination of harmonics in a multilevel converter using the theory of symmetric polynomials and resultants; Chiasson, J.N.; Tolbert, L.M.;McKenzie, K.J.; Zhong Du; Control Systems Technology, IEEE Transactions on, Volume 13, Issue 2, Mar 2005 Page(s):216 – 223.
11. Jose Inacio Leon Galvin, “Multilevel converters: Topoligies, modeeling, space vector modulation techniques & optimization” thesis report.
12. J. Rodriguez , J. S. Lai and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications", IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724-738, 2002
13. R. Teodorescu , F. Beaabjerg , J. K. Pedersen , E. Cengelci , S. U. Sulistijo , B. O. Woo and P. Enjeti, "Multilevel converters—A survey", Proc. EPE Conf., pp. 2-11, 1999
14. A. Nabae , I. Takahashi and H. Akagi, "A new neutral-point clamped pwm inverter", IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518-523, 1981
15. S. K. Mondal , J. O. P. Pinto and B. K. Bose, "A neural-network-based space-vector pwm controller for a three-level voltage-fed inverter induction motor drive", IEEE Trans. Power Electron., vol. 38, no. 3, pp. 660-669, 2002

AUTHORS PROFILE

R. Jayachandra, has obtained his M.Tech degree from JNTU hyderabad. He has more than10 years of teaching experience. He published 4 research papers at National & International level. He is presently a research scholar at JNTUH,Hyderabad., Telangana. He is working in the area of FACTS Controllers & Algorithms.

Prof. G. Tulasi Ram Das, has obtained his M.E from Osmania university and Ph.D from IIT Madras. He has more than 30 years of teaching experience. He has published 151 research papers at National and International level. His research area is Industrial Drives, FACTs devices.Telangana, India.