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Minimization of SIDELOBE Attenuation and Power of a Fir Low Pass Filter using FRFT and CSD Algorithm

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***Abstract:** For digital signal processing, communication systems and VLSI design architectures, an efficient FIR filter is required to eliminate the noise signals. To design an efficient FIR filter, the minimization of two parameters is required such as side lobe attenuation and power. These two parameters can be achieved by designing a FIR filter with the help of Fractional Fourier Transform (FrFT) and Canonical Signed digit (CSD) algorithm. In this work, Finite Impulse Response (FIR) low pass filter is designed by using both FrFT and ordinary Fourier Transform (FT) methods and their frequency responses are compared in terms of side lobe attenuation (SLA). After comparison of both methods, the better results are obtained for an FrFT based design of FIR low pass filter. Apart from this, the FrFT based design of FIR low pass filter is realized in direct form architecture and implemented in VLSI. Further, the Canonical Signed digit (CSD) algorithm is applied for the multiplication process in the architecture implementation to minimize the power consumption. Moreover, frequency response of FIR low pass filter is obtained by using MATLAB software and simulation and synthesis results are obtained by using Xilinx 13.1 ISE.*

***Keywords:** FIR filter, Fourier Transform, FrFT, CSD Algorithm, Double precision floating point format, Q format*

I. INTRODUCTION

FIR filter is mostly used in signal detection in RADAR, pulse shaping, SONAR and equalization of communication channels because of its linear phase characteristics. The Fractional Fourier Transform (FrFT) is a generalization of the classical Fourier Transform and it was used many years ago to solve the differential equation in quantum mechanics and optics. The main advantage of Fractional Fourier Transform (FrFT) is to change the filter response by changing the parameter 'a'. In addition to this, the side lobe attenuation can be minimized by changing the parameter 'a'. In the design of FIR filter, multipliers are the critical elements and occupy more space and consume more power. It is necessary to minimize the power by applying the some power reduction algorithms. Canonical Signed digit (CSD) algorithm is the most efficient algorithm to obtain the power consumption. Before applying the CSD algorithm to minimize the power consumption of filter, first the filter coefficients are represented in double precision floating point format and then Q-format. The FRFT is defined with the help of design equations and transformation angle kernel Ka (t,u).The main controlling parameter in FrFT is 'a'.

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$$K_\alpha(t,u) = \begin{cases} \partial(t-u) \ \text{if } \alpha \text{ is a multiple of } 2\pi \\ \partial(t+u) \ \text{if } \alpha+\pi \text{ is a multiple of } 2\pi \\ \sqrt{\frac{1-j\cot\alpha}{2\pi}} \ \text{if } \alpha \text{ is not a multiple of } 2\pi \end{cases} \quad (1)$$

$$X_\alpha(u) = \int_{-\infty}^{\infty} x(t)\, K_\alpha(t,u)\,dt \quad (2)$$

$$X_\alpha(u) = \int_{-\infty}^{\infty} x(t)\, K_\alpha(t,u)\,dt$$

$$X_\alpha(u) = \begin{cases} \sqrt{\frac{1-j\cot\alpha}{2\pi}}\, e^{j(u^2\cot\alpha/2)} \int_{-\infty}^{\infty} x(t)\, e^{j\left(\frac{t^2\cot\alpha}{2}\right)-jut\operatorname{cosec}\alpha}\,dt; \\ \qquad \text{if } \alpha \text{ is not a multiple of } 2\pi \\ x(t); \ \text{if } \alpha \text{ is a multiple of } 2\pi \\ x(-t); \ \text{if } \alpha+\pi \text{ is a multiple of } 2\pi \end{cases} \quad (3)$$

Here, α=aπ/2.By varying the parameter 'a', which varies 'α', the side lobe attenuation of FIR filter varies. Generally the coefficients of the filter are represented in double precision floating point arithmetic. To represent the floating point numbers, The Qn.m format is used and which is standard method for representing N-bit numbers. Canonical Signed digit is a radix 2 signed digit coding and it uses digits 1, 0 and -1.The Canonical Signed digit algorithm consists of three properties such as no two consecutive bits in Canonical signed digit representation of a number are non zero, the Canonical signed digit representation of a number uses a minimum number of non zero digits and the Canonical signed digit representation of a number is unique. By using the string property, a number can be represented repeatedly in canonical signed representation. In a string of bits, first move from left to right and 1 is taken as $\bar{1}$and it represents -1 and the rest of the bits are considered as 0's.This process is repeated until to get no strings of 1's in the given number. The bit '1' represents consumes power and '0' represents consumes no power.

II. LITERATURE REVIEW

The FIR filter is designed using various window techniques based on the FrFT and FT methods. Less ripples are obtained in the pass band by using FrFT method [1]. FIR low pass filter has been designed by using rectangular window and FrFT method. Based on the FrFT method, the better magnitude response was obtained and side lobe attenuation is reduced to low level [2].FIR low pass filter is designed based on the Genetic algorithm and FrFT method. Using these techniques, the side lobe attenuation has been increased from -28.31dB to -32.07dB for control parameter of '0.95' of FrFT [3].

For a fixed time delay, the signal to noise ratio changes based on the changing the parameter ‘a’ of FrFT [4].The FIR low pass filter was designed using Bohnmon window based on the FrFT method for eliminating the power line interference in ECG signal [5]. From the literature review, it is concluded that there are no power reduction methods for FIR low pass filter with FrFT. In this paper, both side lobe attenuation and power of a FIR low pass are minimized.

III. PROPOSED METHOD

First of all, FIR filter is designed based on required specifications such as using Fractional Fourier Transform and Fourier Transform techniques. After designing a FIR low pass filter, the frequency response is compared in terms of side lobe attenuation. After comparison, Fractional Fourier Transform based FIR low pass filter is implemented in direct form structure. After this, the filter coefficients are represented in double precision floating format and then Q-format representation. After this, Q-format number is represented in binary form. Apply the canonical signed digit algorithm to the bits to minimize the power consumption. Finally the simulation, synthesis and power reports are obtained using XILINX13.1ISE.

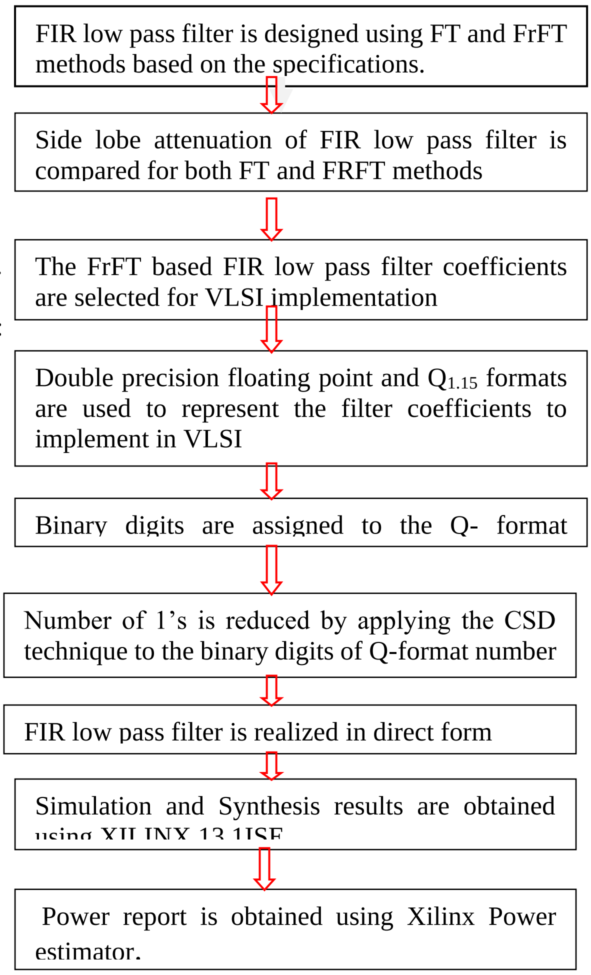

Fig.1. Flowchart of proposed method

IV. RESULTS AND DISCUSSIONS

The FrFT based FIR low pass filter is designed based on the Specifications such as cut-off frequency is 0.5π rad/sec, Order of the filter (N) is 15 and ‘a’ is 0.2 .In addition to this, the hamming window is used to design a FIR low pass filter.

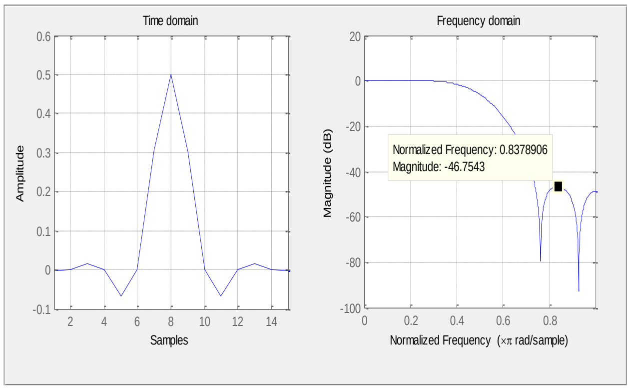

Fig.2. Time domain and Frequency responses of FIR low pass filter using hamming window based on FT method.

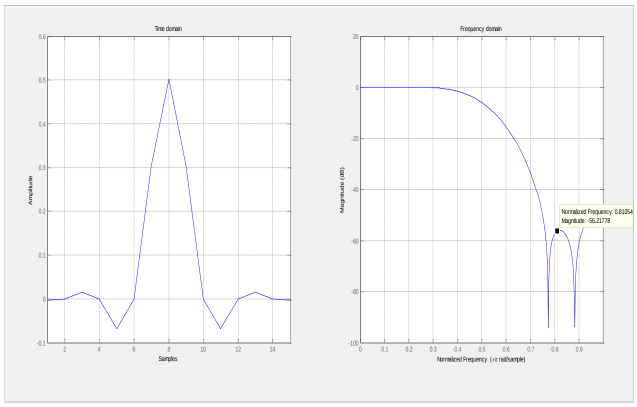

Fig.3.Time domain and Frequency responses of FIR low pass filter using hamming window based on FrFTT method and ‘a’= 0.1.

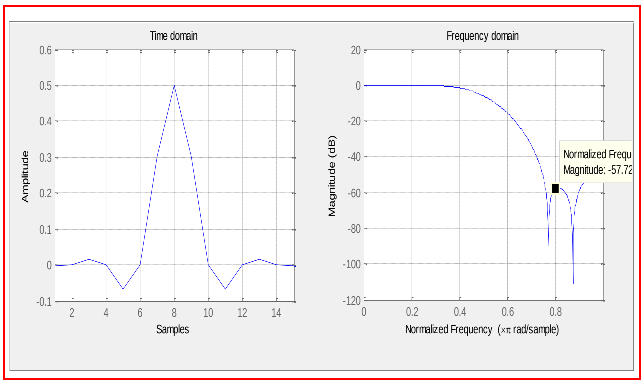

Fig.4. Time domain and Frequency responses of FIR low pass filter using hamming window based on FrFTT method and ‘a’= 0.2.

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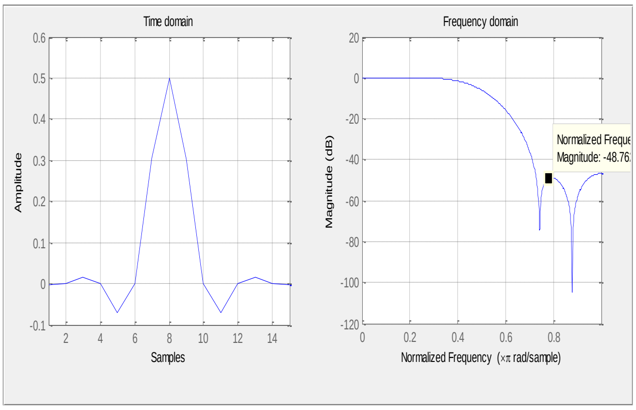


Fig.5. Time domain and Frequency responses of FIR low pass filter using hamming window based on FrFT methodand 'a'= 0.5.

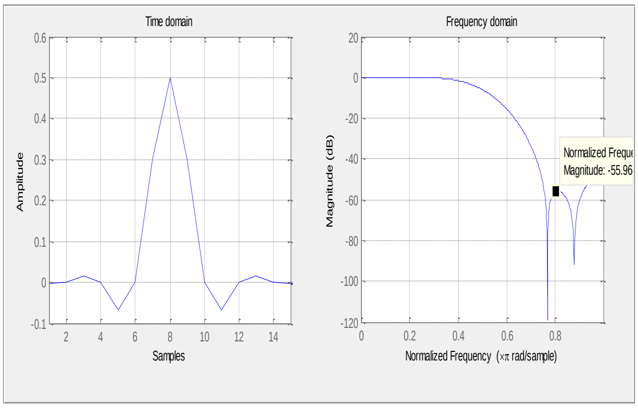


Fig.6. Time domain and Frequency responses of FIR low pass filter using hamming window based on FrFT method and 'a'= 0.8.

Table1: Side lobe attenuation of FrFT based FIR filter for various values of 'a'

Parameter 'a'	Relative side lobe attenuation
0.1	-56.11821
0.2	**-57.28645**
0.3	-40.5344
0.4	-37.85363
0.5	-48.45515
0.6	-45.47094
0.7	-47.30107
0.71	-46.88876
0.72	-46.85502
0.799	-55.75676
0.8	-55.73625
0.9	-56.08506
1	-46.78463

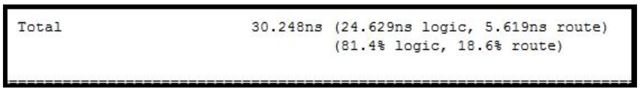
Table2: Comparison of Side lobe attenuation of FrFT and FT based FIR low pass filters

Method	Side lobe attenuation(dB)
FRFT based FIR low pass filter for 'a'= 0.2	**-57.28645**
FT based FIR low pass filter	-46.7543

Table3: FIR filter coefficients

h(n)	h(n)* 2^{15}	Binary values	CSD values
h(0) = 0.5010	16417	0010000000100001	0010000000100001
h(1) = 0.3029	9922	0001011011000010	$0010\bar{1}00\bar{1}0\bar{1}000010$
h(2) = -0.0002	-7	0000000000000111	$000000000000100\bar{1}$
h(3) = -0.0678	-2225	0000100010110001	$00000101\bar{1}\ 0\bar{1}0001$
h(4) = 0.0001	3	0000000000000011	$000000000000010\bar{1}$
h(5) = 0.0158	521	0000000100001000	0000000100001000
h(6) = -0.0000	-0	0000000000000000	0000000000000000
h(7) = -0.0026	-88	0000000001011000	$000000010\bar{1}0\bar{1}0000$

Fig.7.Simulation result of 15 tap FrFT based FIR LPF with binary representation of coefficients.



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Total                     30.248ns (24.629ns logic, 5.619ns route)
                                    (81.4% logic, 18.6% route)
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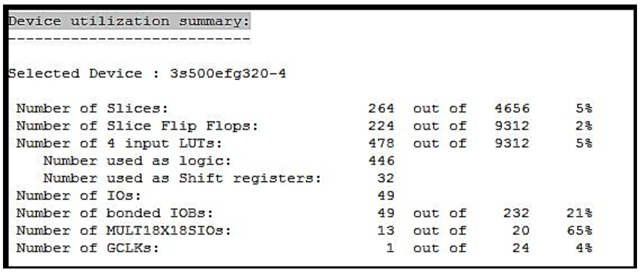
Fig.8. Delay report of 15 tap FrFT based FIR LPF with binary representation of coefficients.



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Device utilization summary:
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Selected Device : 3s500efg320-4

 Number of Slices:                      264  out of   4656     5%
 Number of Slice Flip Flops:            224  out of   9312     2%
 Number of 4 input LUTs:                478  out of   9312     5%
    Number used as logic:               446
    Number used as Shift registers:      32
 Number of IOs:                          49
 Number of bonded IOBs:                  49  out of    232    21%
 Number of MULT18X18SIOs:                13  out of     20    65%
 Number of GCLKs:                         1  out of     24     4%
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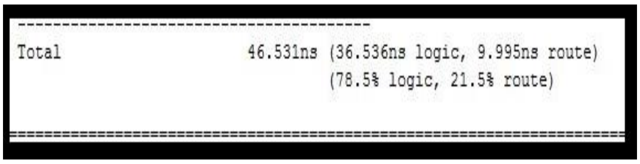
Fig.9. Synthesis report of 15 tap FRFT based FIR LPF with binary representation of coefficients.



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Total                     46.531ns (36.536ns logic, 9.995ns route)
                                    (78.5% logic, 21.5% route)
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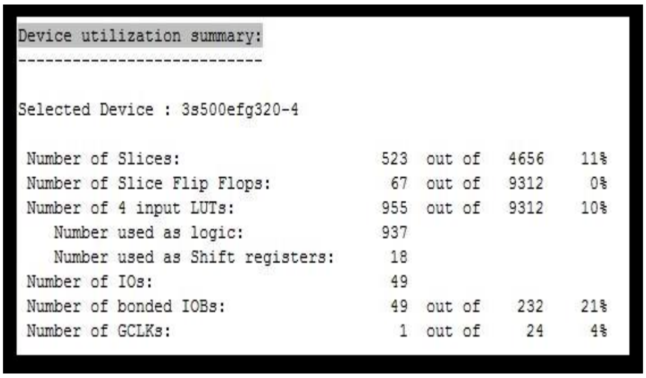
Fig.10. Delay report of 15 tap FrFT based FIR LPF with CSD representation of coefficients

Fig.11.Simulation result of 15 tap FRFT based FIR LPF with CSD representation of coefficients.



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Device utilization summary:
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Selected Device : 3s500efg320-4

 Number of Slices:                      523  out of   4656    11%
 Number of Slice Flip Flops:             67  out of   9312     0%
 Number of 4 input LUTs:                955  out of   9312    10%
    Number used as logic:               937
    Number used as Shift registers:      18
 Number of IOs:                          49
 Number of bonded IOBs:                  49  out of    232    21%
 Number of GCLKs:                         1  out of     24     4%
```

Fig.12. Synthesis report of 15 tap FRFT based FIR LPF with CSD representation of coefficients.

Table4: Performance comparison in terms of power consumption.

Representation of coefficients	Power(mW)
Binary	374
CSD	297

The figures 2 to 6 shows the response of FIR low pass filter with FT and FrFT using MATLAB window visualization tool for N=15.The table 1 shows that the side lobe attenuation of FrFT based FIR low pass filter. From this table, it is observed that maximum side lobe attenuation is obtained at ‘a’ = 0.2.

When the FrFT based FIR low pass f filter is compared with FT based FIR low pass filter in terms of side lobe attenuation, the FrFT based FIR low pass filter gave good results by the parameter ‘a’.VLSI implementation of FrFT based FIR low pass filter is carried out using XILINX 13.1 ISE. The 15-tap FrFT based FIR filter with a=0.2is realized in direct structure and the filter coefficients are implemented using binary and CSD representation. The table3 shows the filter coefficients in such as Q1.15 format, binary and CSD. Simulation, synthesis and implementation of design done by using the Xilinx Integrated Software Environment (ISE) and Verilog language is used for coding. Simulation, power and delay reports of filter with binary and CSD representations are shown in figures7 to 12. Table 4 shows that filter using CSD consumes less power when compared with binary representation.

IV. CONCLUSION AND FUTURE SCOPE

It is concluded that an efficient FIR low pass filter has been designed by using Fractional Fourier Transform method and its side lobe attenuation was obtained as -57.28645dB when compared to the ordinary Fourier transform method.After designing, the filter is implanted in VLSI architecture with the help of double precision floating format and Q- format. After implementing, power is estimated using binary representation method and CSD algorithm method.77mW power is reduced for a FIR low pass filter by using CSD algorithm when compared to the binary representation method. When multiplying two 16-bit numbers such as input and coefficient then more number of partial products will be generated. The future scope of this work is to use any partial product reduction technique to obtain further less power consumption.

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