International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9 Issue-5, March 2020

Implementation of Sensor Precision Mirror Rate using FPGA

Anusha. K, Chinnaiah. M. C, Divya Vani. G, Kishore Vennela, Mudasar Basha

Abstract: ***The research contribution is increasing in the field of autonomous spacecraft. The major role contributes to the navigation methods for spacecraft. The intended control design is required precision mirror rate sensor (PMRS) to maintain positioning and stability of the satellite. One major drawback of the PMRS resides in the lock in effect, by which the sensor is not capable of sensing the rotation at low inertial angular rates. In the proposed work due to the uniqueness, it is able to sense the rotation even at the low inertial angular rates. The frequency control loop has been designed, it generates the resonance frequency using dither motor. The frequency control loop of the PMRS, is developed using a 32 bit MICROBLAZE soft core processor along with PID algorithm and same is executed using Xilinx Spartan 6 FPGA.***

Keywords **: *PMRS(precision mirror rate sensor), lock-in effect, Dither, PID controller.***

I. INTRODUCTION

To control the orientation in flight, gyroscopes are required for the Guidance, navigation and control systems for both in spacecrafts and aircrafts. Especially, in order to control and stabilize the altitude of the satellite, the measurement of the angular motion is essential. Systems employing a gyroscope including control and processing electronics to provide the most direct method for sensing inertial angular velocity.

In inertial navigation systems, which use gyroscopes to measure rate of rotation and acceleration. The measurements are integrated once or twice to yield position. The advantage of inertial navigation systems are self-contained. Besides, inertial sensor data drifts with time and it need to integrate rate data to yield position, small amount of error increases without bound after integration. Equipment cost is high and it is one of the problem with inertial navigation systems.

For example, highly accurate gyros, used in airplanes, are prohibitively expensive. Now a days, recent laser gyrosare very precise, have become more attractive as alternative solutions because of their lower cost.

The dither resonant frequency control loop is evolved on SPARTAN-6 FPGA [11]. The most cost efficient FPGAs are the Spartan-6, which are offering prominent connectivity features such as high logic-to-pin ratios, various number of supported I/O protocols and small form factor packaging.The devices are built on 45nm technology, ideally suited for a range of advanced bridging applications found in automotive infotainment, consumer, and industrial automation. The advantages of Spartan-6 includes 45nm Process Node, best-in-class cost, power, performance, High-speed I/O and MicroBlaze Processor Design Kit.

The next section of the paper is organized as follows: Section II with Related work, section III proposed algorithm and next followed with result and conclusion.

Revised Manuscript Received on March 30, 2020.

***** Correspondence Author

Anusha.K*, ECE, B.V.R.I.T, Narsapur, Medak, INDIA. Email: anusha.kaligota@bvrit.ac.in

M.C Chinnaaiah, ECE, B.V.R.I.T, Narsapur, Medak, INDIA.. Email: chinnaaiah.mc@bvrit.ac.in

Divya vani.. G, ECE, B.V.R.I.T, Narsapur,b Medak, INDIA. Email:divyavani.g@bvrit.ac.in

Kishore Vennela, ECE, B.V.R.I.T, Narsapur, Medak, INDIA. Email: anusha.kaligota@bvrit.ac.in

Mudasar Basha, ECE, B.V.R.I.T, Narsapur, Medak, INDIA. Email: anusha.kaligota@bvrit.ac.in

II. LITERATURE SURVEY

The Precision Mirror Rate sensor (PMRS) can be used to measure angular rotation with high accuracy and precision. One of the significant limitations of PMRS is lock-in effect. At some condition, the difference in distance travelled by the two laser beams will be equal to zero, resulting in the two waves oscillating at the same frequency. This effect is described as lock-in[3], at this condition the Precision Rate sensor(PMRS) not being capable of sensing rotation at low inertial angular rates.

The gyro rotates in one direction and the opposite. Mostly, the gyro is working far from the lock-in region. The dither is driven by its motor. The dither mechanism is essentially a torsional spring assembly which is piezoelectrically driven at its natural frequency. To improve the dither drive efficiency, the dither drive signal must enable the block of the laser gyro to oscillate at the resonant frequency of the dither motor. The function of the dither control systemis to maintain desired angle displacement and track the resonant frequency of the dither motor. The role of the dither control system is to sustain and track the resonant frequency of the dither motor. In the last dither control method, a piezoelectric transducer (PZT) is commonly used to sense the angular displacement of the gyro block as the dither feedback [4],[5]. But the PZT has hysteresis and switching characteristics, and the sensitivity of PZT always changes with time. As the sensitivity of PZT changes with time, the feedback voltage from the transducer does not reflect the real dither status [6], [7].So, a new dither control system is developed using PID controller. PID controller [8] is used for controlling the dither frequency. PID controller is One of the most common controlling methods. The parameters of the PID controller are KP, KI and KD that provide satisfactory closed-loop performance. The parameters[9] speed, response, settling time and proper overshoot rate, will guarantee the system stability to be satisfied.

The MicroBlaze processor is a 32-bit RISC soft processor core which is highly configurable and can be used as embedded processor in FPGAs.[10] or the microcontroller.

III. DESIGN METHODOLOGY

A. Block Diagram

The proposed algorithm is developing dither resonant frequency control loop for PMR sensor. The design implemented on SPARTAN-6 FPGA which consists of inbuilt MicroBlazeprocessor, by which only one board can be used instead of using separate board for processor. Here dither resonant frequency control loop has been designed by interfacing FPGA with processor through AXI.

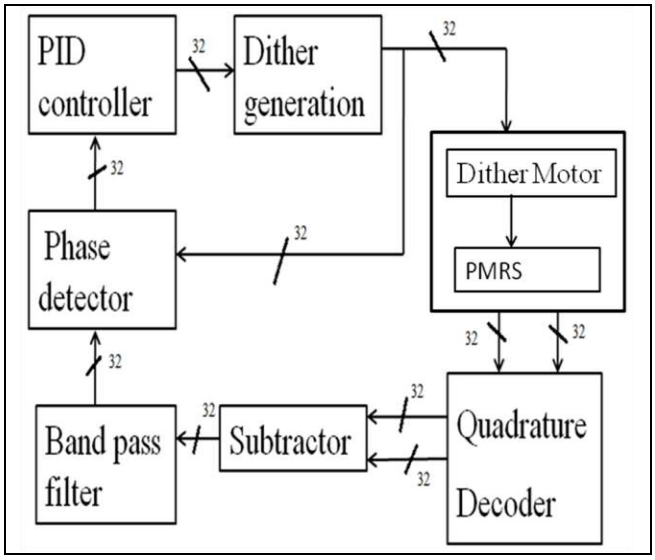

Fig:1 . Block diagram of new dither resonant frequency control loop

A. PMR Block Dither Motor:

The read-out signal of PMR sensor is the beat frequency of the counter propagating laser beams which is sensed by photodiode and produces analog sine and cos signals. The block diagram of new dither resonant frequency control loop is as shown in the Fig.1.

The first step in processing the signals is to find the number of times the signals cross the zero line. The ZCD is thus essentially a squaring circuit. The module detects the point at which the sample value changes from a positive value to a negative value. At that point, it generates a low value and retains the low value until the signals change from the negative value to the positive values.

B. Quadrature Decoder:

The TTL pulses obtained by the ZCD is given as input to the quadrature decoder. The quadrature decoder is one of the phase detection mechanism which is a crucial part of the signal processing. The quadrature decoder decodes information from the sin and cos signals. when the sin is leading the cos signal, quadrature decoder produces positive direction and when the sin is lagging the cos signal, it produces negative direction. The positive direction is denoted by one and negative direction as zero. The outputs of the quadrature decoder are the direction signal and the pulses. In the quadrature decoder a pulse value should be generated for both the falling as well as the rising edge of both sin and cos signals. In order to produce pulse for each edge of the sin and cos signals, the sin and cos signals are xored with their delayed version.

The next step in the process is to count the number of pulses for every 100μs and is viewed in the Labview. These counts gets registered in two different registers Counter A and Counter B.

For every 100μs the count value is reset to zero and it again starts counting. For this purpose, interrupt is generated and is given to the processor. Here the external interrupt is generated and is given to the interrupt of processor. The steps for passing the count value to the labview are as follows.

- Generation of the interrupt in the processor
- Reading the value of the count in to GPIO in the processor.
- Send the value of the GPIO to UART and is viewed in the labview.

1.Generation of the interrupt in the processor:
The external interrupt is given to the interrupt pin in the processor and the interrupt is enabled by following steps.

a) Initialize the interrupt: the interrupt has been initialized.
b) Master enable: enable all interrupts in the Master Enable register of the interrupt controller.
c) Enable interrupt:enable individual interrupts in the interrupt controller.
d) Microblaze enable interrupt: enable interrupts on the MicroBlaze system. When the MicroBlaze processor starts up, interrupts are disabled. Interrupts must be explicitly turned on.
e) Device driver handler : This function is the primary interrupt handler for the driver. It must be connected to the interrupt source such that is called when an interrupt of the interrupt controller is active. It will resolve which interrupts are active and enabled and call the appropriate interrupt handler.

2.Send the value of the GPIO to UART:
The value of the GPIO is send to the UART by following steps.

a) Initialize the send buffer and receive buffer of UART
b) Send the data present in the send buffer.

The detailed block diagram of dither frequency control loop interfacing with the processor is as shown in the Fig.2.

The number of pulses in the positive direction is registered in register Counter A and the number of pulses in the negative direction is registered in the register Counter B.

C.Subtractor:

The output of Counter A and Counter B subtracted from each other. The so obtained count corresponds to both dither component and the actual rotation to be measured. The dither component has all information about the dither, such as amplitude and frequency. Here we are concentrating on only dither so as to acquire only dither component, the subtracted output is passed through the IIR Band Pass filter (BPF).

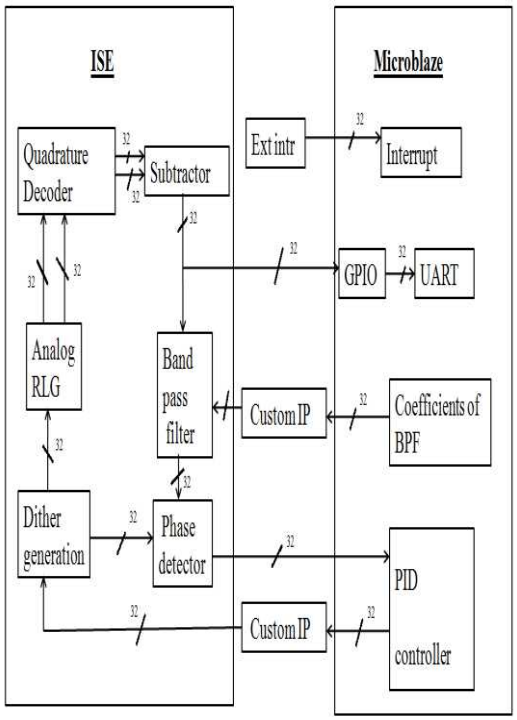

Fig.2.The detailed block diagram of dither frequency control loop interfacing with the Microblaze

D.IIR Band Pass filter (BPF):

The IIR filter is a non-recursive filter where in present output depends on present input, past inputs and past outputs. The BPF passes certain band of frequencies of the signal and rejects the other band of frequencies of the signal. Normally, the dither frequency ranges from 300Hz-500Hz. So, the BPF is designed in such a way that it passes only this range of frequency signals. The equation for the biquad IIR filter is as follows

$Y(n) = \sum_{k=0}^{N} a_k x(n-k) + \sum_{k=1}^{M} b_k y(n-k)$…. (1)

Where Y(n) is the present output,ak and bk are the coefficients, x(n-k) are the input samples and y(n-k) are the past output samples.

The coefficients of the BPF are generated in the processor and is passed to the BPF by creating custom logic by the following steps.

- Create/import peripheral
- Selecting the no of registers
- Customizing the peripheral
- Adding the custom peripheral to the system

E. Phase Detector:

The output of the BPF is passed to the phase detector. The phase detector compares the phases of output of the BPF and input of the dither motor. If the phase difference is 900 the dither motor is working at resonant frequency.

F.Proportional-integral-derivative (PID) controller:

The PID controller controls the resonant frequency by phase difference.The PID controller is one of the most common controlling methods in the market. In industrial control systems, a Proportional-integral-derivative (PID) controller is a control loop feedback mechanism which is commonly used. A PID constantly calculates an error value e(t) as the difference between set point and a measured process variable. The controller attempts to minimize the error overtime by adjust of a control variable. A block diagram of PID controller in a feedback loop is shown in the Fig.3.

Equation of PID controller is as follows

$U(t)\{\displaystyle u(t)\}=KP\ e(t)+Ki\ \int_{t0}\ e(t)\ dt+Kd\ \frac{d\ e(t)}{dt}$…(2)

where KP, Ki, and Kd all are non-negative, denotes the coefficients for the proportional, integral and derivative terms respectively (sometimes denoted as P,I and D). Thecommonly used terms to describe the PID control loops, are as:

Control Variable (CV) – it is the output of the control loop. Here, the CV is the frequency produced by the PID controller.

Process Variable (PV) – it is the feedback value returned by the system to the controller.In this case, the PV is the current phase, which is the output of phase detector.

Set Point (SP) – Set point is the value that we desire for the system. In our case, the SP is the target phase is 900.

Error (E) – Error refers to the difference between the set point and the process variable. In another words, it means how far the current phase from the target phase. From the block diagram of PID controller, we can see that the output of the loop is merely the sum of output from P, I and D controller.

The equations for the PID loop are illustrated below:

Last Error = Error (3)
Error = Set Point – Process Variable (4)
Integral = Integral + Error (5)
Derivative = Error – Last Error (6)
*Control Variable = (Kp * Error) + (Ki * Integral) + (Kd * Derivative) (7)*

If the phase difference is greater than or less than 90^0 the PID controller increases or decreases the frequency of the dither motor and controls the dither motor to work at resonant frequency. The output of PID controller is given to dither generation. Depending upon the output of PID controller the frequency of dither generation changes.

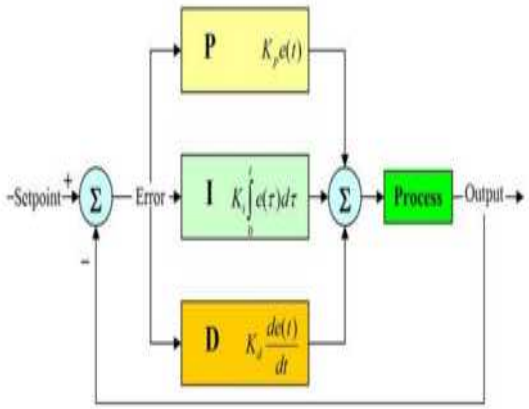

Fig.3. A block diagram of PID controller

G.Dither Generator:

The dither generator produces two signals DD1 and DD2, which are 1800 out of phase. The frequency and the pulse width can be adjusted in order to make the dither motor to work at resonant frequency. The DD1 and DD2 signals are subtracted and a quasi-squarewave is generated. This signal is amplified to 48v peak to peak by the power amplifier and is used to drive the dither motor.

The flowchart for dither frequency control loop is as shown in the fig.4.

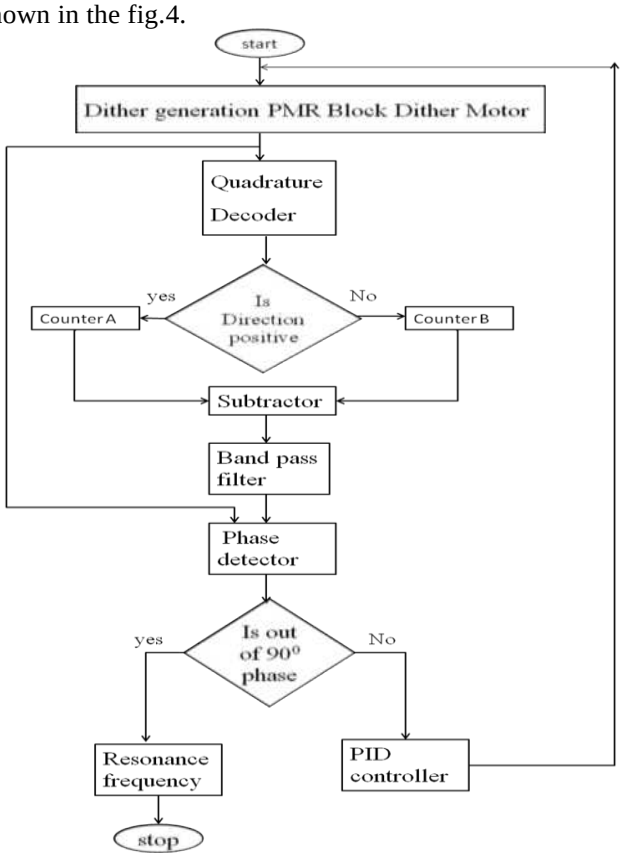

Fig.4. The flowchart for dither frequency control loop

Flowchart Steps:

1) The PMR block produces sin and cos signals and is passed to quadrature decoder.
2) The quadrature decoder produces direction based on sin and cos pulses and the number of pulses.
3) If the direction is positive the number of pulses are counted in counter-A and If the direction is negative the number of pulses are counted in counter-B.
4) The outputs of both counter A and B are assed to the subtractor.
5) The subtracted value is passed to the Band pass filter.
6) The output of Band pass filter and dither generated output is passed to the phase detector to detect the phase difference between them.
7) If the phase difference is 90^0 then the PMR block is working on the resonant frequency of dither motor.
8) If the phase difference is not 90^0then the PMR block is not working on the resonant frequency of dither motor and hence it is passed to the PID controller.
9) The PID controller generateses frequency based on the phase differences, which is given as the input to the dither generation block and makes the PMR block work on the resonant frequency of dither motor.

IV. SIMULATION RESULTS

The simulation results of Algorithm are shown below. The simulation results of Quadrature decoder is shown in Fig.5.

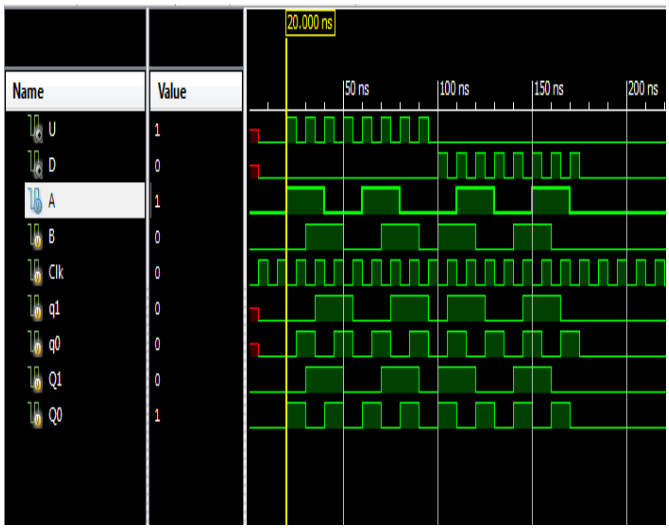

Figure 5. Simulation results of Quadrature decoder

The simulation results of Quadrature decoder results is shown in Fig 5.1.In the Fig.5.1.the inputs are the TTL pulses of sin and cos from Zero Crossing Detector and outputs are U and D pulses.when sin leading cos that is 1 and 0 then the outputs is 1, when cos leading sin that is 0 and 1 then the outputs is 0. For example when A is '0' and B is '0' U is '1' and D is '0'. when A is '1' and B is '0' U is '1' and D is '0'. when A is '1' and B is '1' U is '1' and D is '0'. when A is '1' and B is '1' U is '1' and D is '0'. when A is '0' and B is '1' U is '0' and D is '1'.i.e when A leading B the output is 1, when B leading A the output is 0.

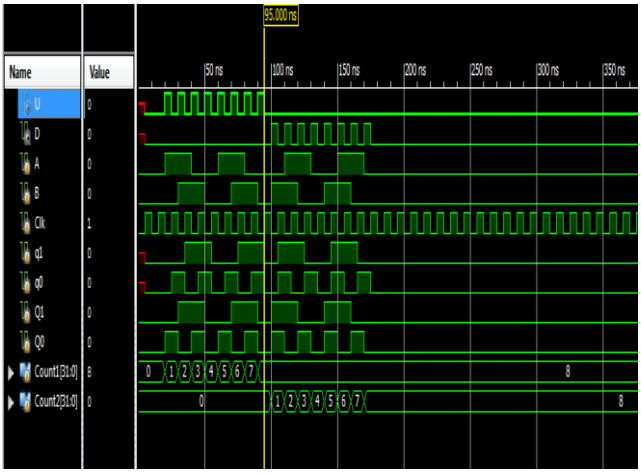

Fig.6. The simulation results of Counter

From the Fig.6. the number of positive pulses in the quadrature decoder are given to counter1 and the number of negative pulses in the quadrature decoder are given to counter2. The outputs of countr1 and counter2 are given to subtractor. Whenever U is '1' and D is '0' then the counter 1 is counted. Whenever D is '1' and U is '0' then the counter 2 is counted.

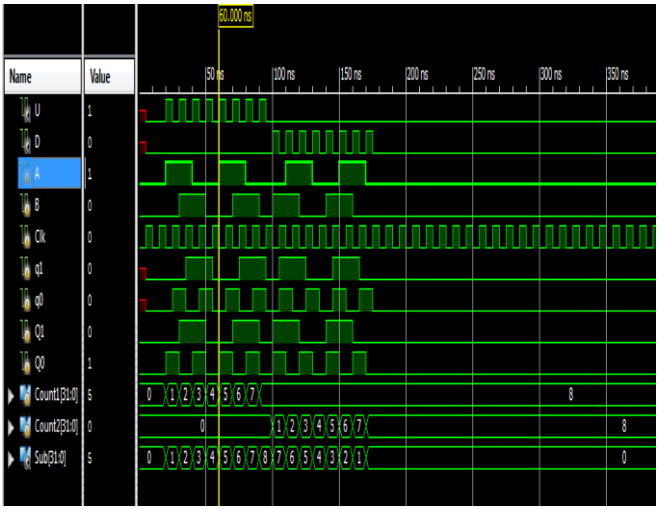

Fig.7. The simulation results of subtractor

The input to the subtractor is Counter1 and Counter2.The count values from counter1 and counter2 are subtracted,then the resultant value is Subtractor output.
The simulation results of dither generation is shown in fig 7. In the Fig.7.the inputs are the frequency and the pulse width, according to that dd1 and dd2 output signals are produced.

V. SYNTHESIS REPORT

xc6slx9-2-csg324	Used	Available	Utilization
Slice registers	366	11440	3%
DSP48A1s	6	16	37%
Slice latches	270	5720	4%

The synthesis report is shown in the above table. In this design the number of multipliers for bi-quad IIR Band pass filter has been reduced to 2.The number of slice registers used are 366 out of 11440.The number of DSP48A1s are 6 out of 16 and the number of slice latches are 270 out of 5720.

VI. CONCLUSION

This paper discusses about design and development of the algorithm on SPARTAN-6 FPGA which consists of inbuilt MICROBLAZE processor. This system is used in navigation and guidance and control systems to maintain orientation in flights. The dither resonant frequency control loop has been designed by using PID controller.

REFERENCES

1. M. Faucheux, D. Fayoux, J. J. Roland "The Ring Laser Gyro " J. Optics (Paris), 1988, vol. 19, no 3, pp. 101-115.
2. Joseph E.Killpatrick,Dale Berndt "Modular Laser Gyro"U.S 6208414,2001.
3. Chow WW. The ring laser gyro. Review of Modern Physics 1985;57:61–104.
4. Fritze KR. "Laser gyro dither drive" U.S. Patent 5225889; 1993.
5. Killpatrick JE. Dither control system for a ring laser gyro. U.S. Patent 6476918; 2002.
6. ZhenfangFan,HuiLuon,GuangfengLu,ShaominHu,"Direct dither control without external feedback for ring laser gyro", Optics & Laser Technology,2011.
7. Guangfeng Lu,* Hui Luo, and ZhenFang Fan, "Dither-frequency-track method based on phase sensitive detector technology in mechanically dithered ring laser gyros",Proc. of SPIE Vol. 8418,2012.
8. Daya Sagar Sahu, Sunil Sharma, "A Survey Paper on PID Control System" International Journal of Engineering Trends and Technology (IJETT) – Volume 21 Number 7 – March 2015.
9. Nayak, et al., STUDY OF TUNING OF PID CONTROLLER BY USING PARTICLE SWARM OPTIMIZATION International Journal of Advanced Engineering Research and Studies,2015.
10. Vaibhav Kale, "Using the MicroBlaze Processor to Accelerate Cost-Sensitive Embedded System Development"White Paper: MicroBlaze™ Embedded Processor.
11. Maureen Smerdon "Spartan-6 FPGAs:performance,power,and i/o optimized for cost-sensitive applications" White Paper: Spartan-6 FPGAs.

AUTHORS PROFILE

Anusha.K, Received M.Tech degree from Jawaharlal Nehru Technological University Hyderabad. Currently she is working as an Assistant Professor in BVRIT Narsapur. Her Area of Interest in VLSI Design.

M.C Chinnaiah, Received the Ph.D. degree from Jawaharlal Nehru Technological University Hyderabad. where he is currently a Professor. He was a Visiting faculty member for CDAC Hyderabad. He was working in the field of VLSI and automation systems.

Divya Vani.G, pursuing her Ph.D from KL University, vijayawada , Andhrapradesh. Currently she is working as an Assistant Professor in BVRIT Narsapur. She is working in the field of VLSI and Robotics.

Kishore Vennela, pursuing his Ph.D from KL University, vijayawada , Andhrapradesh , India. He is working in the field of VLSI and Robotics and associated with DST funded project on service robotics. His contributions mainly focus on autonomous robotics specifically, service robots for indoor applications. He has publications in the stream of VLSI based robotics and his field of interest is robotics and sensor networks. Currently he is working with team that focus on the human assisting robots in the indoor locations.

Mudasar Basha, working as an Assistant professor in BV Raju Institute of Technology, Narsapur, Telangana. He is pursuing Ph.D from Koneru Lakshmaiah Educational Foundation (KLEF), Vijayawada, Andhra Pradesh, India. He completed his M-Tech from JNTU Anantapur affiliated engineering college. His area of interest includes VLSI, Microprocessors and currently he is working in the field of VLSI and Robotics. He is an active Professional member **of** Institute for Engineering Research and Publication (IFERP).