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A Versatile Design of Low Power and High-Speed Operational Amplifier using Nano Scale Transistors

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Abstract: ***This paper illustrates the design of low power and high-speed operational Amplifier using Nanoscale Transistors. The proposed design introduces biasing block, for generating I=10uA for Channel length=180nm Technology. Adding biasing block to two-stages operational Amplifier current is constant i.e. there are no fluctuations in power supply, increase in bandwidth and power dissipation is less as compared the previous result. The design is simulated in p-spice tool and performed AC analysis. After analysis, the design achieved the parameter like Gain = 40db, Phase Margin=90º, Unity Gain Band Width=13MHz, Output Swing=0.1v to 1.7v and Power Dissipation=0.145mW.***

Keywords **: *Operational Amplifier, Unity Gain Bandwidth, Gain, Phase Margin, Output swing, Power Dissipation***

I. INTRODUCTION

In the present technology, CMOS technology has rapidly increased in the domain of analog integrated mixed-mode signal circuit by providing less cost, highly reliable, low power and high performance circuits. One of the significance challenges for designing a low power application is channel length reduction.

Operational Amplifier is one of the fundamental blocks in Analog IC Technology. Generally, it is a DC-coupled voltage differential amplifier; the majority of them are single Bandwidth demanding Applications Single-stage Amplifiers are insufficient to drive. To enhance the gain and Bandwidth, Two-stage Amplifiers have been used. Constant Thrust for innovation motivated me to explore the characteristics of an op-amp. The objective is to design an Analog ASIC (Two-stage op-amp) in 180nm Technology. The most important requirement of an operational amplifier is to have substantial open-loop gain, to implement magnitude and gain ended output. Usually, it generates an output voltage, which is a million times greater than the voltage difference provided by its input terminals. To attain the large Gain and High bandwidth negative feedback concept has been used. To overcome instability while applying negative feedback, the frequency response of this circuit must be shaped appropriately by considering a frequency compensation technique. Numerous techniques are proposed to stabilize closed-loop two-stage amplifiers [1][2]. For a specific quantity of power consumption, each one of these method makes an excellent trade-off between the bandwidth and stability. In Miller compensation technique [3], the compensation capacitor is positioned in between the input, and output of the second stage. It has pole splitting action that moves from one pole to lower frequencies and the other pole moves to higher frequencies, which enhances the closed-loop stability but reduces the bandwidth. The issue is less power efficiency low power supply rejection ratio and feed-forward current flows through the compensation capacitor. The current which produces in the right half-plane is zero, which impacts on closed-loop stability. To enhance the stability of the designed two-stage amplifier, cascade compensation technique has been used.

The first stage consists of differential pair PMOS with current mirrors of NMOS and Second stage made up of CS amplifier. Sizes for the lengths are typically 1.5 to 10 times of the minimum amount length (whereas present digital circuits frequently use the minimum). For an ideal operational amplifier Differential voltage gain is infinite, the input resistance is infinite, and output resistance is zero.

The paper has been structured as follows, Section II describes regarding Literature survey of this paper. The Section III describes about proposed design specification for two-stage operational amplifier, and Section IV is about simulation results, Section V representing about comparison between exist design, and proposed design, and Section VI represents the Conclusion and future work.

II. LITERATURE SURVEY

In paper[4] Ketan. J. Raut represented the design of two-stage op-amp using standard 180nm technology and achieved the parameter. Open loop gain of the amplifier is 74.89db, bandwidth is 7.3MHZ, and Phase Margin is 48º with 10pf capacitive and 1M ohm Resistive load. The average power consumption of the amplifier is 0.402mW, and the Slew Rate is 10V/µs. The Voltage is 1.8V.

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Akhil Gupta, [5] designed a specification of 1.8V with 50uA bias current by producing gain higher than 66dB, the slew rate of 95V/ µs. By reducing the current, the gain can increase, but the slew rate is condensed, which affects the sensitivity of the amplifier. Power consumption is also reduced by reducing the size of the MOSFET. Hassan Khameh, Hossein Shamsi et al. [6][7] approached positive feedback and gate driven method to design two-stage op-amp using 180nm technology. By contacting this, he can increase DC gain upto 20dB, but unity-gain bandwidth of the op-amp remains same. The settling time is demonstrated by applying op-amp in a flip around the sample and holds the circuit and proved that his design has better settling time than its conventional counterpart.

M.D Abdullah- et al. [8] designed low power, low voltage, small offset, and high speed two-stage CMOS op-amp achieves gain as 60.24db, 1.4ns settling time, 8.4mv offset voltage. The Supply voltage is +1.8V to -1.8V with 1.15mW power.

Ehsan Kargaran et al. [9] approached the cascade technique to increase the dc gain and miller capacitor feedback path to enhance the unity gain bandwidth, but the power dissipation of the circuit is 50 MW and provides different responses with different temperature.

Varsha Bendre et al. [10] Presents a performance analysis of two-stage trans-conductance operational amplifier considering conventional gate driven mode using TSMC 180nm technology. From analysis settling time has been 472ns slew rate is achieved 0.37V/ µs, output swing around 1.25V, power dissipation is 536.5 µW, and supply voltage is 1.8V.

Chaitali et al. [11] designed for biomedical applications in which all the transistors are operated for low voltage low power applications' using in TSMC 180nm technology and simulation has done in the Cadence environment. The circuit generates 40db gain, 114KHZ UGB, 72deg phase margin, power dissipation is112nW with 0.8V battery.should be less than 5%.

III. DESIGN METHODOLOGY

A. Block Diagram

The designed two-stage operational amplifier circuit consists of four blocks, namely biasing circuit, differential amplifier circuit, compensation circuit, and high gain stage. The aim of this design is to meet all of the design specifications successfully.

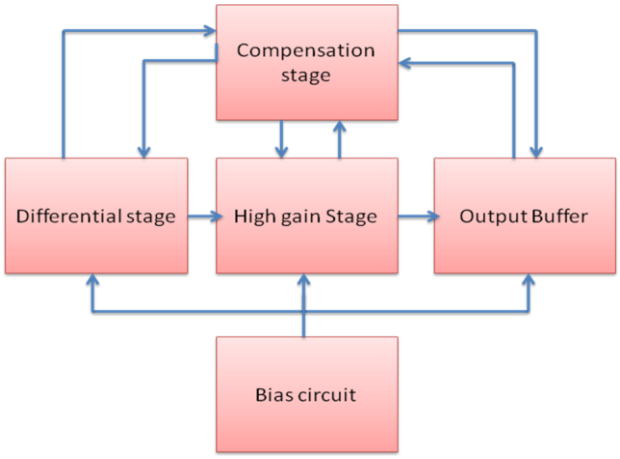

Fig: 3.1 Block diagram of 2 stage op amp

Bias circuitry: The function of bias circuit is to supply constant DC voltage at its gate terminals; this voltage is used to recognize ideal current sources for biasing the current sink of a differential amplifier. It is a self-biased circuit, as shown in figure 3, which does not require any input voltages. Current flowing through the transistors decides the node voltages. The purpose of the source resistance is to maintain consistent current in both the branches so that their node voltages are constant irrespective of power supply variations. The dimensions (W and L) of the transistor are chosen in such a way that the required current flows through the transistors. The current through the biasing circuit is decided by the current needed to bias the op-amp. 10uA is the biasing current in our op-amp design, so the biasing course is also designed for 10uA.

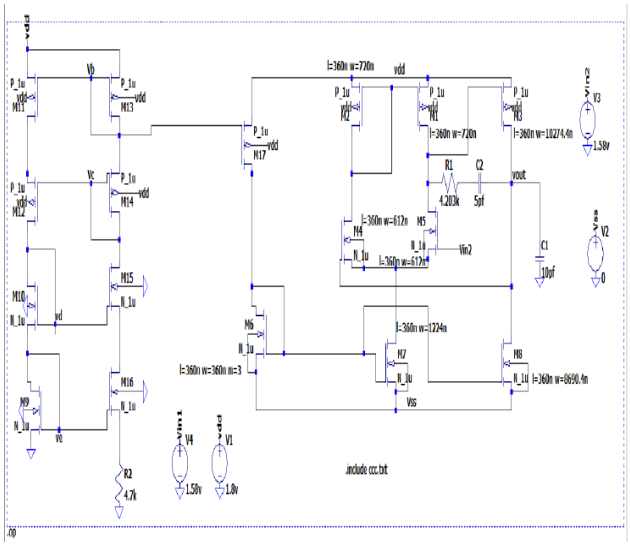

Fig:3.2 schematic of 2 stage operational amplifier

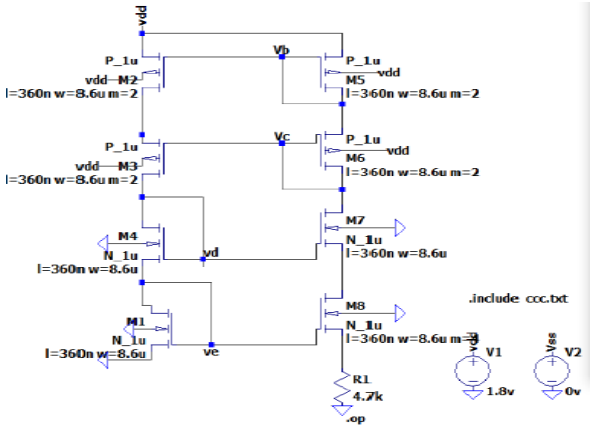

Fig:3.3 Biasing block of 2 stage operational amplifier

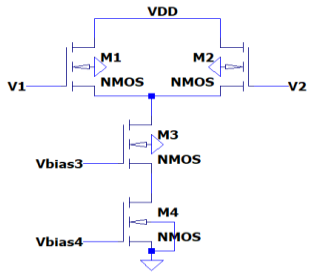

Fig:3.4 Differential amplifier of 2 stage operational amplifier

Differential Amplifier: It is an input phase that exists in approximately all op-amp circuits. It discards the common-mode signals and amplifies differential signals to achieve higher gain from the single stage, as shown in figure 3.2 The same principle is used to cancel out common-mode input noise.

Compensation circuit: It consists of a compensation capacitor which is used to improving gain for bandwidth. Generally, feedback capacitor is used to connect between input and outputs terminals of a Common Source Amplifier, which helps in reducing the gain at higher frequencies to stabilize the frequency response.

High Gain stage: The gain from the single stage is not sufficient enough, so the second stage is added to increase the overall gain of an op-amp. It helps in improving output swing, as well.

Output Buffer: Ideally on-chip op-amps drive only capacitive loads that are not needed in most of the cases. The purpose of this output buffer is to reduce the loading effect. Commercially available discrete op-amps require output buffers to drive off-chip loads.

B. Design Specifications

The design specification and parameters are shown in the tabular column

Table-I:Specification of the design

Parameters		Value
V_{dd}	Drain Voltage	1.8 v
V_{ss}	Source Voltage	0v
GB	Gain Bandwidth	13MH_z
C_L	Load Capacitances	10PF
ICMR Max	Maximum Common mode input range	1.58
ICMR Min	Minimum Common mode input range	0.7
ϕ	Phase angle	65°
P_{diss}	Power Dissipation	<=2mW
A_v	Voltage gain	40db
SR	Slew rate	10v/μs
V_{out}	Output voltage	0v to 1.8 v

C. Theoretical Calculations and Implementation

The design method starts by selecting a device length, which will determine channel length modulation lambda. To calculate the power dissipation of a designed specification, dc simulation is to be performed for both minimum and maximum ICMR value.

$$\text{Vin(max)} = V_{DD} - \sqrt{\frac{I_7}{\beta_2}} - |V_{TO2}|\ (\text{max}) + |V_{T1}|\ (\text{min}) \quad (1)$$

Negative ICMR:

$$\text{Vin (min)} = V_{SS} - \sqrt{\frac{I_7}{\beta_1}} - |V_{T1}|(\text{max}) + \text{Vds5} \quad (2)$$

$$\text{Slew rate SR} = \frac{I5}{Cc} \quad (3)$$

To obtain phase margin of 60^o have to select appropriate C_c values as 2.85 times C_L.

$$C_c > \frac{2.85}{10} C_L \quad (4)$$

$$C_c > \frac{2.85}{10} \text{ *10pf } (C_L = 10\text{pf}) \quad (5)$$

$$C_c > 2.85\ \text{pf} \quad (6)$$

Since I_7 is the sink current of differential amplifier it is depend on slew rate and it is to be calculated by equation 7 by choosing C_c value =5pf I_7 =10µA

$$I_7 = \text{SR} * C_c \quad (7)$$

=10µA

$$I_2 = \frac{1}{2}(I_7) \quad (8)$$

The transistor M2 is connected PMOS current source & M1 is its mirror. Next $\left(\frac{W}{L}\right)_2$ is calculated by using I_7 ICMR(Max) equation hence .

$$\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_1 \quad (9)$$

Next have to calculate Gm trans conductance

$$\text{Gm1=GBW } *2\pi * C_C \quad (10)$$

$=62.8\mu$

The Dc gain is directly related to Gm2 and bandwidth is expressed as

$$\text{GBW} = \frac{0.45\ Gm2}{Cc} \quad (11)$$

By increasing $\left(\frac{W}{L}\right)_5$ Dc gain and gain bandwidth decreases.

M4 (inv) & M5 (Non-inv) are the diff pair NMOS input transistors. So $\left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_5$

$\left(\frac{W}{L}\right)_4$ is calculated using Gm1 & I_7 .

$\left(\frac{W}{L}\right)_4$ =1.7

Vds7 is calculated from Negative ICMR Vds7=0.06v

M7 is the sink of diff amp

$\left(\frac{W}{L}\right)_7$ is calculated by using I_7 and Vds7

Gm3 ≥ 10 (12)

Gm4 =628µ (13)

Gm1=$\sqrt{2\beta I_D}$=44 (14)

$S_3 = S_1 \frac{Gm3}{Gm1}$ (15)

($S_3 = \left(\frac{W}{L}\right)_3$, $S_1 = \left(\frac{W}{L}\right)_1$) (16)

=28.54

$I_3$is calculated using Gm3, k3 and S_3

I_3= 71µA , $\left(\frac{W}{L}\right)_7 = \frac{I_3}{I_7}\left(\frac{W}{L}\right)_8$ (17)

M8 is the nmos of second stage op amp

$\left(\frac{W}{L}\right)_8$ =24.14.

Calculating Gain and Power dissipation

$P_{diss}=(I_5+I_6)(V_{dd}+V_{ss})$ (18)

Simulating circuit and verifying the result to meet required specification.

IV. SIMULATION RESULTS

The simulation results represent AC analysis of two stage amplifier.

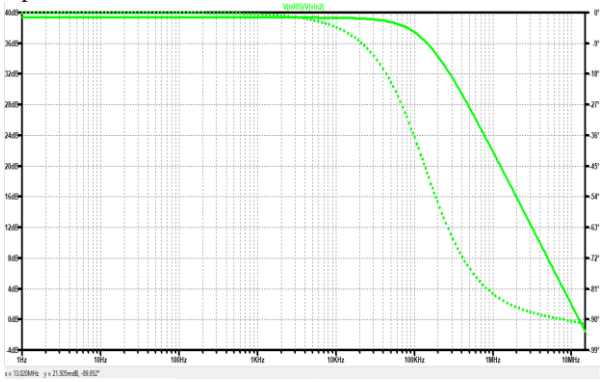

Fig:4.1 AC analysis of Two stage amplifier

From the Fig 4.1 the observed values are as follows by supplying 1mv input to the circuit and performing AC Analysis the proposed design achieved gain=40db and phase margin=89º and bandwidth=13MHZ .

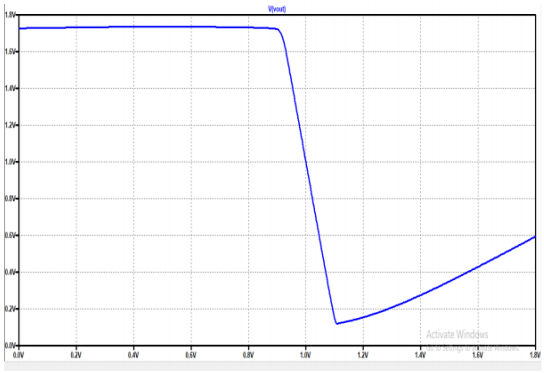

Fig:4.2 output swing

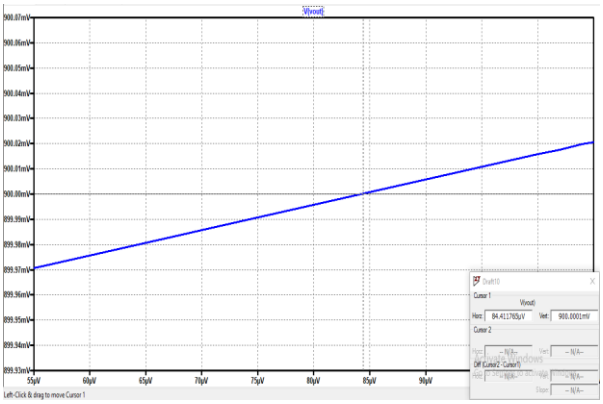

Fig:4.3Offset Voltage

The specification of output swing is based on change in the small signal gain with the change in the DC output level. Defining small signal gain by assume that the output is at 0V to 1.8V DC level. But the range is around +0.1v to 1.7v

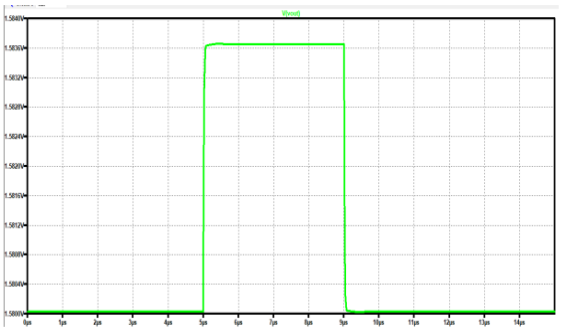

Fig:4.4 Rise time and Fall time

Figure 4.3 represents Rise time and Fall time, it has been calculated by using dv/dt equation from graph there is increase in rise time from 10% to 90% of its maximum value and fall time that is 90% to 10% of minimum value.

V. COMPARISION TABLE

The comparison between the existence method and the proposed method of two-stage operational amplifier. The UGB is enhanced from 7.3 MHz to 13MHz i.e. 78% is increased, and Phase margin is increased around 87 %, and Power dissipation is increased up to 25 %.

Table-II: Comparision between exist and proposed method

Specification	Exist method	Proposed method
UGB	7.3MHz	13MHz
Phase margin	48º	90º
Power dissipation	0.402mW	0.145mWs

VI. RESULT AND DISCUSSION

The proposed work designed a low power and high-speed operational amplifier using nanoscale transistors.
Initially, biasing block has been designed for generating I=10uA by choosing Channel length=180nm, such that there are no fluctuations in power supply and also to implement the current source on-chip, that designed biasing block circuit is connected to low power and high-speed operational amplifier and performed Ac analysis. The obtained results in different parameters like Gain=40db, Phase Margin=90degrees, Unity Gain Band Width=13MHZ, Output Swing=0.1v to 1.7v, and Power Dissipation=0.145mW using LT Spice tool. Performed all the theoretical calculations required for calculating all the above parameters to achieve the design specification. An application of low power and high-speed op-amp power consumption is less and bandwidth is improved. The future work can enhance by varying W/L ratio which leads to reduce the channel length.

VII. CONCLUSION

The proposed work designed a low power and high-speed operational amplifier using nanos ale transistors. Initially, biasing block has been designed for generating I=10uA by choosing Channel length=180nm, such
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