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Edge Triggered Clock with Mtcmos Level Shifter Design for Soc Applications

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Abstract: ***Level shifter is used to communicate between low core voltage to high input and output voltage. It is an interfacing component between two voltages. Level Shifter enters between different modules for voltage communication without using any additional pin. To minimize power consumption due to different supply voltages in the level shifter circuits, voltage shifting from low to above threshold. MTCMOS is used in this technique along with edge triggered flip flop. In this technique the predicted power consumption reached below 1.5mW from the conventional power consumption. Using Different power supply predicted power consumption is achieved in this Technique.***

Key word: ***level shifter, mtcmos, predicted power consumption, different power supply in different voltage domain. edge triggered flip flop.***

I. INTRODUCTION

In SoC Applications, Power consumption is the major issues placed in day by day Challenges. The Techniques used to reduce power consumption among the literature, MTCMOS Technique with different supply voltage has taken the major role to reduce the power consumption and also used to reduce the leakage of power. The increase complexity of SoC's needed low power consumption. The reduction in leakage current in general purpose application such as wireless mobile and internet , phone, tablet etc. The technique used for multi supply voltage domain consists of partition of circuit into separate voltage. Higher supply voltage run for Time Critical domain circuit and Lower supply voltage run for low critical domain circuit. Voltage Island, MTCMOS Technique is used in this domain. To improve power efficiency Time-Critical Domains Run At Higher Power Supply Voltage (Vddh) and Non-Critical Sections Work At Lower Power Supply Voltage (Vddl).

II. TECHNIQUES USED

- **System On a Chip:**

Integrated all components in a single chip is system on chip. The typical applications are Embedded system power supply. Partition of domain in separate voltage domain

- **Voltage Islands:**

Depending on the timing requirement each voltage domain is operated at proper power supply. Partition of domain in separate voltage domain

- **Level Shifter**

There is a circuit linkage between low voltage domain to high voltage domain. Interconnection between two component.

Logic Level.

In general digital circuit, Boolean logic is used. Binary 0 corresponds to logic low and Binary 1 corresponds to logic 1.The Range of Voltage depends on each level of the circuit. Logic level is usually determined voltage difference between signal and ground.

MTCMOS

In Order to Optimize Delay and Power, MTCMOS Technique is used for high efficient. A transistor with multiple threshold voltage normally referred as MTCMOS Technique

A Low Vth Devices act as switch Faster. It is used to minimize clock period and critical path delay.A High Vth is Used to reduce static leakage power .

III. LITERATURE REVIEW

Chi, J.C. et al.(Jun.2007) proposed a voltage scaling with multiple supply is used for low power designs. The algorithm used a approaches greedy algorithm and an improving interative optimization is used.

Lütkemeier,S. & Rückert,U.(Sep 2010) proposed a novel level shifter circuit is used for converting subthreshold to above-threshold signal levels. In Other existing implementations it is required a flow of static current and it is offer considerable static power savings.

IV. DCVS LEVEL SHIFTER DESIGN

DCVS circuit is used to connect the MP2 AND MN2 transistors. We need to properly balanced the circuit, the strength of the circuit is needed. The DCVS-LS behaves as a ratioed circuit for pull up and pull down network for proper balancing the circuit.

In Order to reduce static and dynamic power consumption, use blocks with different supply voltages in different circuit or in different paths within one single block .

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Gates working with the higher supply voltage have better speed performance at the cost of increase power consumption. Hence the high supply voltage should only be used. The function of effective alternative to a D flip-flop can be used dynamic circuits and flip flop.
The addition of edge triggered D flip flop with level shifter as long as it is clocked often enough; while not a true flip-flop, it is act as a
functional role.

V. DCVS LEVEL SHIFTER

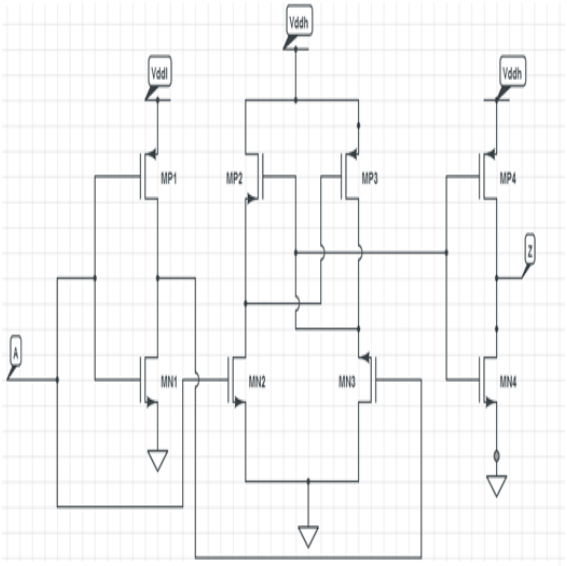

Fig: 1.DCVS LEVEL SHIFTER

When two devices have different supply voltage, voltage-level translation is required**.** Here MTCMOS Technique is used**.** To reduce the leakage and power consumption and to reduce the sub threshold leakage.

To balance the low power to high power level shifter circuit used greatly.

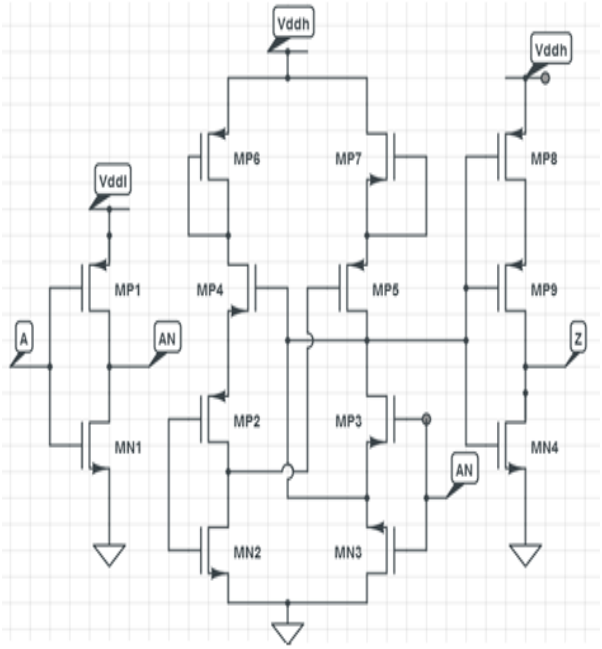

Fig. 2. MTCMOS Level Shifter Design

VI. POTENTIAL PROBLEMS WITHOUT VOLTAGE-LEVEL TRANSLATION

The Condition required are:

1. The circuit with higher-voltage may be needed to drive a circuit with low- voltage
2. The circuit with low voltage device may be needed to drive a circuit with high voltage devices.

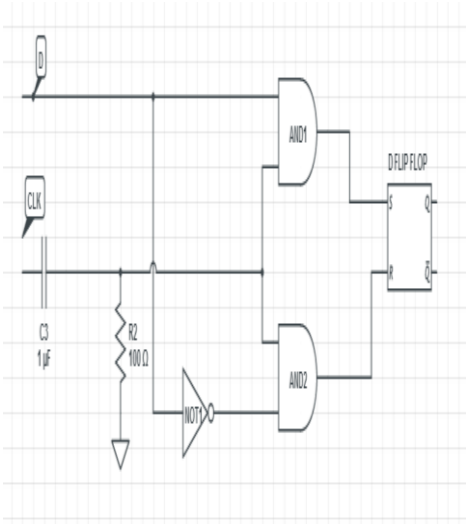

Fig. 3. Advanced method of Edge Triggered clock method is used with level shifter in order to reduce the power

Result :

The Result of the power supply achieved in MTCMOS Level shifter with edge triggered flip flop has 1.5mW**.**

- Edge triggered flip can be connected with level shifter circuit. It can be act as a clock to the circuit. It is able to trigger the voltage from high to low and low to high
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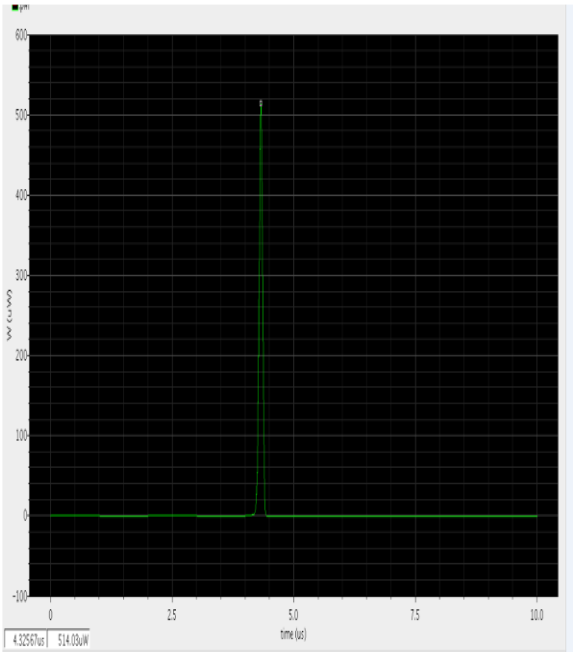

Fig.4. Power Analysis of proposed level shifter design

1.6 Comparison Table:

Table:4.1 COMPARISON OF POWER DISSIPATION

COMPARISON	STATIC POWER
DCVS level shifter	784.2µW
Level shifter with MTCMOS technique	514.0µW
Level Shifter with Edge tiggerd flip flop with MTCMOS Technique	1.5 mW

VII. CONCLUSION

The proposed level shifter circuit with MTCMOS circuit with D flip flop is presented and it is simulated in Cadence Virtuoso tool. The Proposed level shifter circuit wit edge triggered flip flop has has the power consumption upto 1.5mV compared to the conventional level shifter

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Different no of level shifter can be added with future work to improve the efficiency.

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