Design and Implementation of Low Power Delay Locked Loop using Multiplexer Based Phase Frequency Detector

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Abstract*: This paper proposes design and implementation of low power Delay Locked Loop Architecture, with dynamic Multiplexer based Phase Frequency Detector with minimum locking time. Clock and data recovery systems are employed to derive the clocking information to correctly decode the transmitted data at the receiver. Delay Locked Loop is one of the most important clock recovery systems. The DLL architecture is designed using Cadence Virtuoso 180nm Technology with 1.8V power supply. The proposed DLL with Multiplexer based phase frequency detector shows significant reduction in power dissipation by 10% compared to DLL designed using D-FF based PFD and achieves locking state within 10 clock cycles with minimum jitter of 4.84326ps, measured within clock frequency range of 100-250MHz.

Keywords: Delay Locked Loop (DLL); Phase Frequency Detector (PFD); Voltage Controlled Delay Line (VCDL); area; power dissipation.

I. INTRODUCTION

With research and advancement in scaling of CMOS process, there is a huge demand for high speed and highly integrated System on Chip (SOC) to carry out complex tasks. Achieving synchronization between different clock domains is a difficult task as various modules within a SOC may operate at different clock frequencies. Several Clock and Data Recovery systems are employed to achieve clock and phase synchronization. In serial communication systems, clock signal information is not provided along with the transmitted data stream. Hence receiver must employ clock recovery methods to regenerate the clock by utilizing the timing information provided in the transmitted data stream. Clock recovery systems are the most important component of the communication systems like radio, wires and optical fibers. Clock signal information in high speed stream of digital data generated from a disk drive and communication networks like Ethernet is not provided. In such applications, the clock information is generated at the receiver using a reference clock and there by aligning the phase of the clock to the data stream transitions using Clock and Data Recovery methods. Delay Locked Loop is one of the most important systems employed in Clock and Data recovery.

II. DELAY LOCKED LOOP ARCHITECTURE

Delay Locked Loop is a first order non-linear circuit with a negative feedback that adjusts phase of its output clock signal with a reference clock signal. It is used in clock signal synchronization, clock and data recovery systems and clock signal synthesis. The four building blocks in DLL are: Voltage Controlled Delay Line (VCDL), Phase Frequency Detector (PFD), Charge Pump (CP) and Loop Filter (LP), as shown in Figure 1.

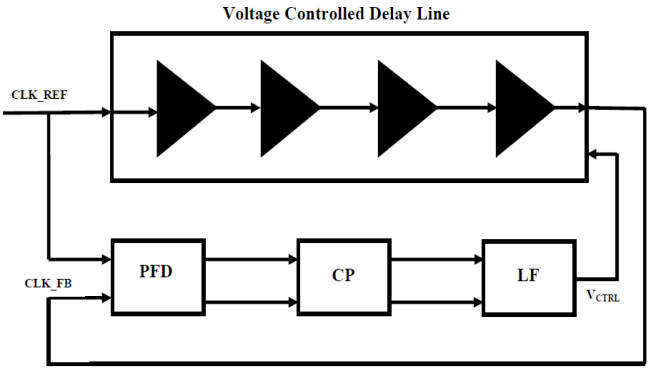

Fig. 1: DLL Block Diagram

The reference clock signal (CLK_REF) is fed to Voltage Controlled Delay Line and Phase frequency detector. The Phase frequency detector generates the voltage pulses indicating the phase error between the reference clock signal and the VCDL output (CLK_FB). These voltage pulses are then provided to the charge pump block as the input. The charge pump converts the output of phase detector into the corresponding error current. This error current is fed to the Loop filter circuit which converts the error current into corresponding voltage change. The loop filter output is provided as control voltage (V_{CTRL}) to the VCDL. The delay in the output of VCDL is directly proportional to the control voltage. Hence VCDL uses the loop filter output as the control voltage to adjust the delay in its output clock signal. This process continues until the feedback clock from the output of VCDL is synchronized with the input reference clock.

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The jitter of the output clock, input clock, VCDL and control voltage are described by equations (1) – (5)

$$\delta_{OUT} \approx \sqrt{\delta^2_{IN} + \delta^2_{VCDL} + \delta^2_{VC}} \quad (1)$$

$$\delta_{IN} = \frac{2\pi * \theta_{IN}}{T_{CLK}} * \sqrt{\frac{1-K_T}{1+K_T} + K^2{}_T} + \delta_{KCLK} \quad (2)$$

$$\delta_{VCDL} = \frac{2\pi}{T_{CLK}} * \frac{\theta_{VCDL}}{\sqrt{1-K^2{}_T}} \quad (3)$$

$$\delta_{VC} = \frac{2\pi}{T_{CLK}} * K_{VCDL} * \Delta_{VC} \quad (4)$$

$$K_T = \frac{2\pi * K_{VCDL} * I_{CP}}{C} \quad (5)$$

Where

δ_{IN}	is the input phase error caused by the signal noise and is the timer error caused by the noise and the slope variation of the clock
θ_{VCDL}	is the VCDL output phase error
Δ_{VC}	Is the voltage noise of the capacitor (C) in loop filter
K_{VCDL}	represents the gain of VCDL in s/V
I_{CP}	is the charge and discharge current in the charge pump

Authors of [1] explain the functional components of DLL and propose a modified VCDL to implement low power DLL. A low power dynamic MUX based PFD is proposed in [2] to reduce jitter and power dissipation. Authors of [3] propose a Phase Locked Loop using modified D-FF based PFD to reduce dead band issue and explain charge pump operation. Dynamic CMOS circuit techniques and its advantages over static designs are explained in [4]. A Phase Locked Loop, using differential VCO, NOR resettable D-FF based PFD is proposed in [5]. Two non-linear PFD architectures are proposed in [6] to eliminate dead zone. A multi-phase DLL is proposed in [7] employing a NAND resettable PFD and VCDL to overcome dead band issues. A comparison of different TSPC configurations of D-FF is carried out in [8]. A high-resolution Time to Digital converter is implemented using an array of Delay Locked Loop in [9] in 0.35µm CMOS process. Reference [10] proposes the implementation of a Delay Locked Loop based Clock and Data Recovery circuit using level tracking technique in Verilog HDL. Reference [11] proposes a high performance phase locked loop designed using 0.18 µm CMOS process based on divider less structure which consumes 13.4mW of power and rms jitter of 3.21 ps. Reference [12] describes spur suppression by reducing current mismatch in charge pump and implements a phase locked loop using 130nm CMOS process with power consumption of 12mW

III. METHODOLOGY

This paper demonstrates the Design and implementation of Delay Locked Loop using D Flip-Flop and Multiplexer based Phase frequency detectors and compares the DLL key performance factors like jitter, locking time, power and area.

A. D-FF based PFD

Fig. 2 below shows the PFD design based on D Flip-flop. The inputs of both the flip flops are connected to the supply voltage VDD and hence it stays at logic one. The reference clock signal (CLK_{ref}) is provided to the input of upper D flip flop while the feedback clock (CLK_{FB}) is connected to the lower D flip flop input. When any of the clock signals switch to logic high, the flip flops will be charged, and output goes high. When both the D flip flop outputs UP and DOWN go high, the AND gate will generate a reset signal to prevent both the D flip flop to produce logic high at the output.

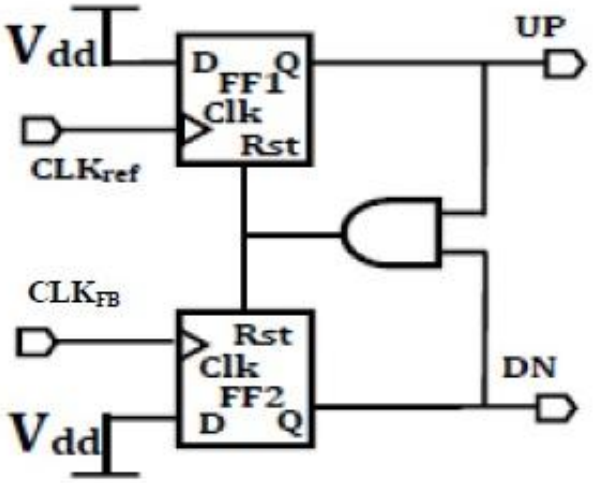

Fig. 2. D-FF based PFD

D-FF based PFD contributes to major portion of power dissipation in the DLL architecture and has large glitch of significant amplitude on the output signals due to the delays associated with reset path which is overcome by dynamic multiplexer-based PFD.

B. Proposed DLL with Dynamic MUX based PFD

The DLL with conventional D-FF based PFD has locking problems due to large glitch in the PFD output. The DLL architecture proposed in this paper uses multiplexer based Dynamic Phase frequency detector [2] to minimize the power dissipation and to reduce jitter in the PFD output signals.

B.1 Low Power Multiplexer based PFD

The low power dynamic PFD is shown in Fig. 3 below. Two multiplexers M0 and M1 are used in this PFD design instead of D flip flops. When CLK_REF signal goes low, transistor C0 is switched ON and the node N1 is charged to supply voltage VDD.

Transistor C1 and C2 hold this charge. Since the MUX select input SEL is connected to CLK_REF, the MUX output UP goes low by selecting MUX input U0. When CLK_REF signal changes to logic high and CLK_FB switches to logic level low, the charge stored at N1 is transferred to the MUX output signal UP by selecting the input U1 and by selecting the MUX input D0, the DOWN signal switches to logic low.

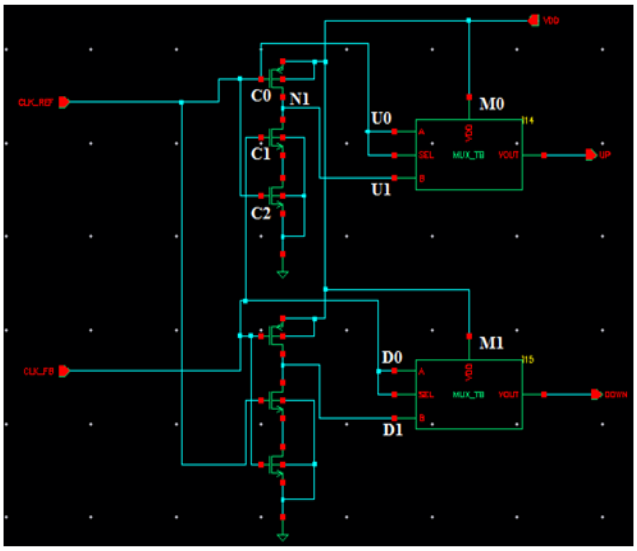

Fig. 3. MUX based Dynamic PFD

B.2 Internal Structure of MUX

The internal schematic of 2:1 multiplexer used in this design is shown in the figure 4. The transistors M1 and M2 form an inverter to invert the signal SEL which controls the transistors M4 and M5. The inverter output signal SELB is used to control the transistors M3 and M6. Transistors M3, M4 and M5, M6 form pass transistors. When select line SEL is low, SELB is high and turn on the transistors M3 and M4 to pass the logic A to the output VOUT. Similarly, when SEL is high, transistors M5 and M6 are turned ON and pass the logic B to output VOUT.

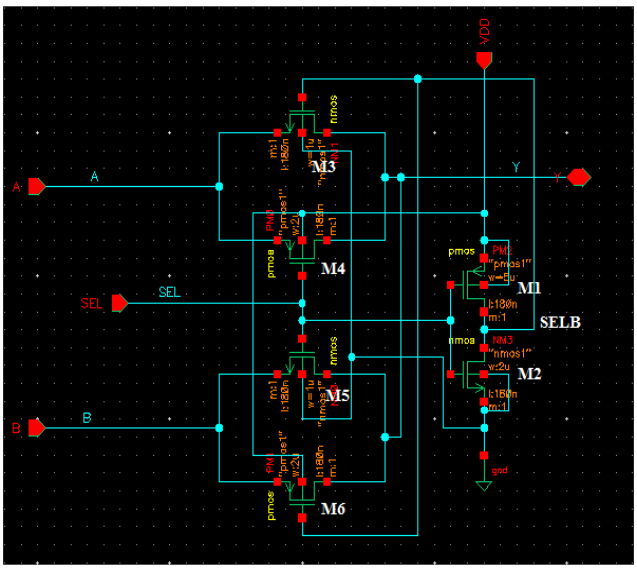

Fig. 4. 2:1 MUX

B.3 Voltage Controlled delay Line (VCDL)

The schematic of the VCDL is shown in Fig. 5 below. Voltage Controlled Delay Line consists of bias circuit, current starved inverters and buffer as shown in below figure 5. The combination of current starved and digital inverters is used to improve rising and falling time of each clock phase. The current mirror circuit determines the current in the delay elements which in turn is determined by the control voltage. The current mirror circuits act as starvation devices.

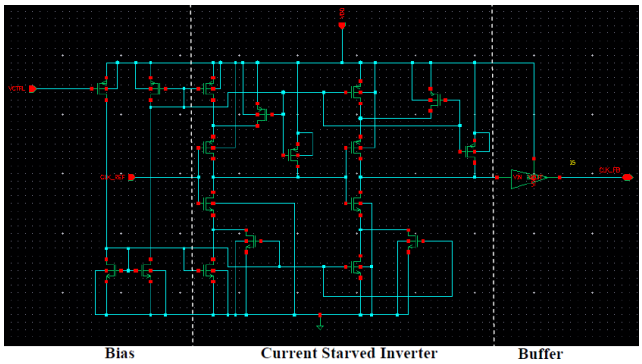

Fig. 5. VCDL Schematic

If the output of the VCDL lags the reference clock signal, then the control voltage is reduced which causes the delay cell current to decrease and hence delay in each delay element will be increased. Finally, this increases the output clock phase time period to match the time period of the reference clock. Hence there will be no variation in the control voltage, thus maintaining the locked state of the delay to the reference clock period and the system is said to be in delay locked state.

B.4 Charge Pump and Loop Filter

The schematic of the charge pump along with loop filter is shown in Fig. 6 below. The charge pump controls the variation in the control voltage by charging and discharging the capacitor depending on the output of the phase frequency detector. Initially, when the reference clock and the feedback clock signals are out of phase, the variation in the control voltage is determined by the charge pump depending upon the UP and DOWN pulses from the output of phase detector, such that feedback clock starts approaching and finally the feedback clock time period is locked to that of reference clock. The charge pump remains relatively stable when the phase difference between both the signals is zero.Charge Pump consists of two switched current sources with load capacitance CP. When a pulse is detected on the DOWN signal line, the capacitor is charged through the PMOS transistor M1. On the other hand, when there is a pulse on the UP signal, the NMOS transistor M2 discharges the capacitor.

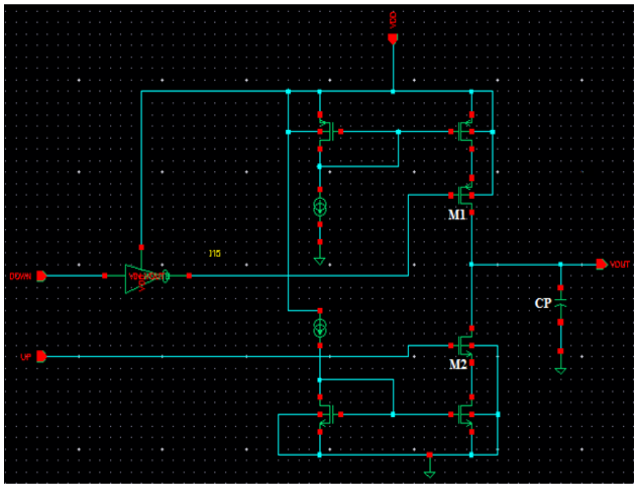

Fig. 6. CP and LP Schematic

IV. RESULT AND DISCUSSION

Figure. 7 below shows the DLL block architecture.

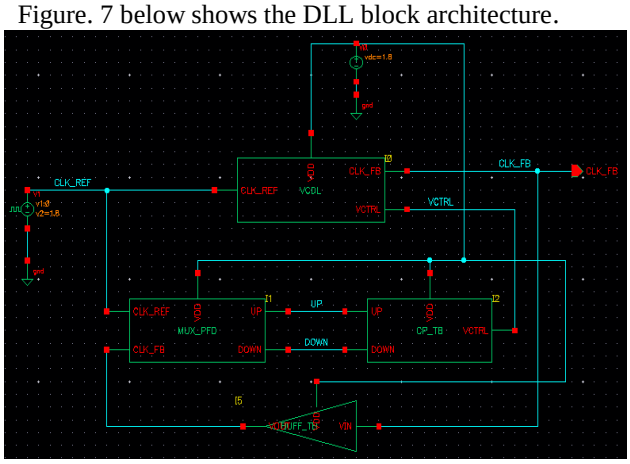

Figure 7: DLL Architecture

The conventional DLL with D-FF based PFD has large glitch of significant amplitude on the DOWN signal line when CLK_REF leads CLK_FB as shown in Fig. 8. But ideally in this case, DOWN signal must be zero, which is not achieved.

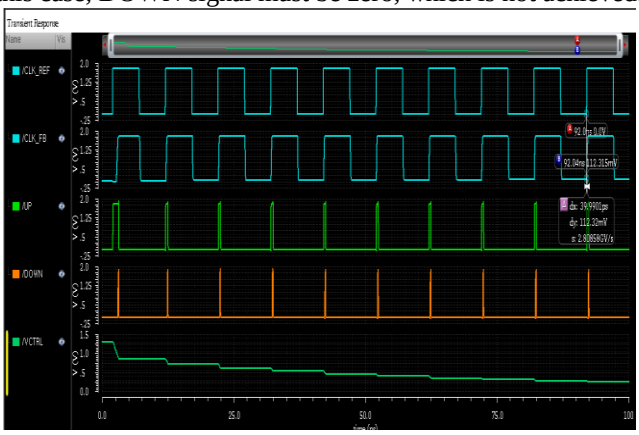

Fig. 8. DLL output with D-FF based PFD

The proposed DLL with dynamic MUX based PFD has DOWN signal with negligible width for the same scenario as shown in Fig. 9.

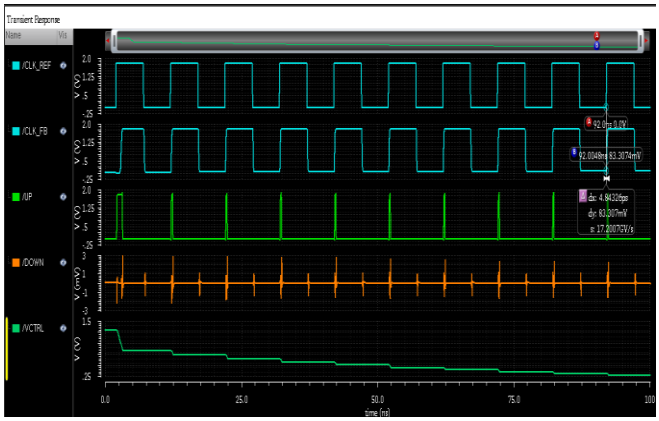

Fig. 9. DLL output using MUX based PFD

The measured jitter of conventional DLL is 39.9901ps with a locking time of 10 clock cycles at a frequency of 100MHz as shown in Fig. 8, while the DLL using MUX based PFD has a jitter of 4.84326ps measured for the same clock frequency with a locking time of 10 clock cycles as shown in Fig. 9

V. CONCLUSION

Delay Locked Loops are the integral part of digital electronics systems used to enhance the timing characteristics of the integrated circuits and clock recovery process for high speed digital communication systems. The DLL with D-FF based PFD has significant jitter of 39.9901ps and DOWN signal of significant amplitude due to reset path delays in the PFD design. The proposed DLL with multiplexer based dynamic DLL overcomes this problem and achieves efficient locking with jitter of 4.84326ps and the measured power dissipation of the proposed DLL is less than that of conventional DLL. Simulation shows 10% reduction in power dissipation.

TABLE I. Performance Comparison

Specification	Proposed Work	[1]	[7]	[9]	[10]
Technology(µm)	0.18	0.13	0.35	0.35	0.35
Supply Voltage(V)	1.8	1.8	2	3.3	3.0-3.6
Frequency Range (MHz)	100-250	60	100	50-120	130-160
Jitter(ps)	4.84326		17.575	7	24
Power Dissipation(mW)	1.83707	0.9215	3.4	23	0.24

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