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An Adaptive Arbitration Technique with 4x4 Mesh Topology for Low Area and High Speed NOC Design

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Abstract: ***In recent days, On-Chip Communication is a major requirement in modern systems that produce efficient communication with less complexity and high throughput. Due to heavy traffic and increasing Network-On Chip (NoC) size, the routing algorithm produces poor performances. Normally, round-robin and matrix arbiters are used in NoC for high-speed switches. In this research work, three different types of arbiter algorithms are used such as priority algorithm, Time Division Multiplexed (TDM) algorithm, and Viterbi algorithm to improve the linearity of the NOC. Initially, the priority algorithm helps to minimize traffic congestion when the arbiter is in a busy mode. Second, the fairness and Quality of Service (QoS) of the NoC structure are analyzed by the TDM algorithm. Finally, the Viterbi algorithm based error prediction process is done in an NoC structure. Due to the usage of three proposed arbiter algorithms, the area of NoC can be reduced. The packet can be reached to the destination by using the arbitration process with less loss. In this research, the proposed methodology is called as Low Area-Fault-Tolerant Adaptive Arbitration based NoC architecture (LA-FTAA- NoC architecture). Finally, the Field Programmable Gate Array (FPGA) performance is evaluated such as LUT, flip flop, slices, and frequency in Spartan 6 hardware. In the proposed method, 2.42% of LUT, 3.1% of flip flop, and 8.63% of slices have reduced when compared to existing work.***

Keywords: Arbiter, Field Programmable Gate Array, Network on Chip, On-chip Communication, Routing Algorithm.

I. INTRODUCTION

As per Moore's law, the number of transistors on a microchip keeps doubling for every couple of years. The System on Chip (SoC) is used to overcome the problem of shrinking chip size in this proposed method. In this way, the Network on Chip (NoC) is introduced to meet the high performance and requirements of the design productivity in communication systems [1]. Presently, the complex SoC has been implemented utilizing new design paradigm NoCs. The data packet is routed by using an efficient algorithm instead of wires [2]. Expressively, the routing scheme influences the performance of the NoC that defines the path of a packet transferred in network architecture. [3] - [5]. Furthermore, the present FPGA's interconnection structure has several shortcomings that poorly affect the performance, limited the FPGA speed, and maximize the communication protocol [6].

The FPGA based NoCs are classified into two types: Soft NoCs and Hard NoCs. Soft NoCs are developed by end-users utilizing traditional FPGA resources. Hard NoCs are embedded blocks that are developed on silicon like other FPGA blocks: embedded Random Access Memory (RAM), embedded processors and multipliers. However, a hard NoC has higher performance compared to soft NoC [7] - [10]. Based on a scalable and very simple architecture platform, the NoC relates memories, processors and other custom architecture design by utilizing packet switching methods on a hop by hop basis. The major aim of this method is to provide high bandwidth and high performance [11]. The NoC attracts and provides higher scalability and enhances the system performance for future SoC compared to traditional bus technology [12]- [14]. In this research, the TDM and Fault Aware Adaptive, QoS and speed based router methods are used to improve the linearity of the NoC. While the routing process, the TDM algorithm is used to minimize or avoid traffic congestion. The performance of the proposed method is analyzed based on FPGA performances: LUT, flip flop, slices, frequency and power.

The rest of this paper is prepared as follows: Reviews the related framework on the low power-aware communication of NoC architectures in section -2. The proposed arbiter NoC architectures are briefly explained in Section-3. Section 4 explains the results and discussion of the proposed method. The research work is concluded in section-5.

II. LITERATURE SURVEY

In the present day, there are several methods used for arbiter algorithms in NoC architecture. This section focuses on reviewing works on NoC and power-aware on-chip communication.

Hassan et al. [15] proposed the NoC Dynamic Partial Reconfiguration (DPR) simulator which was utilized to find limitations and performances of NoC. The NoC based FPGA improved the reconfiguration capabilities due to the performance of several DPRs. Although, supporting several DPR requires to add more resources such as decoupling buffer and Controlling Unit (CU). From this, the reconfiguration time of the DPR with NoC architecture design is best compared to the reconfiguration time of the traditional FPGA platform.

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The number of instantaneous DORs was not exceeded the definite limit for the size of the network.

Chen et al. [16] proposed a path diversity fault-tolerant routing scheme for NoC architecture. The data had only provided a limited view of traffic in the network that output in Heavy Traffic Congestion (HTC). The proposed path diversity fault-tolerant routing scheme used to enhance Fault Resilient Packet Delivery (FRPD) and traffic balancing, which considers buffer information and Path Diversity Information (PDI). The proposed fault algorithm was improved the saturation throughput than conventional methods. This research work not only delivers the packets with the highest path diversity but also has a better capacity to detour from the faulty nodes.

Ezz-Eldin et al. [17] proposed an adjustable delay and congestion aware routing scheme for asynchronous NoC architecture. This scheme has been performed in various adaptive routing schemes with average saturation throughput and delays for different traffic patterns. The proposed Process-variation Delay and Congestion-aware Routing (PDCR) scheme have achieved a 12% to 32% average message delay lower compared to other schemes. Furthermore, this scheme has achieved 11% – 82% of the saturation throughput than other Adaptive Routing Scheme (ARS).

Kawasaki et al. [18] proposed an area-efficient, globally asynchronous NoC architecture for Hard Real-Time Multiprocessor (HRTM) platform. In this paper, the NoC was implemented for message-passing communication between the processor cores, which employs fixed modeled TDM to control the communication through a router structure, network interfaces, and links to provide real-time guarantees. The proposed scheme achieved an efficient area in the NoC architecture by means network interface microarchitecture and asynchronous routers associated with the TDM algorithm. To verify the design, this research has developed a 4 × 4 bitorus NoC in 65 nm CMOS technology and the performance of the proposed scheme was analyzed by area, speed and energy consumption for the router, post layout and NoC.

Wang et al. [19] proposed an efficient design for the test technique of NoC. In this research work, Esy Test and comprehensive test scheme with minimized influence have been proposed to improve the system performance. By using Reconfigurable Router Architecture (RRA) and Adaptive Fault Tolerant Routing (AFTR) scheme, the router has accessed respective information. During the test procedure, all the processing cores performances are maintained properly. At the same time, EsyTest has been provided a full test coverage used for NoC architecture and better hardware usability than existing works.

III. PROPOSED METHODOLOGY

Arbiter is the process of transmitting data packets from source to destination node. The major aim of arbiters is correctness, fairness, and simplicity. The arbiter algorithms are classified as adaptive arbiter algorithm and non- adaptive arbiter algorithm. Adaptive arbiter algorithm changes their arbiter decisions for controlling the traffic congestion in the network topology. This algorithm adjacent the arbiter when one or two nodes are unavailable. Non–adaptive arbiter algorithm does not change its routing decision.

A. Congestion avoid by Priority algorithm

To achieve high throughput, NOC multiplexes the data on the channel and shares the data throughout the network. The packet contention problem in switch results leads to unpredictable delays for each data flow and the contention problem. If the size of the arbiter has increased, the delay of the entire architecture has increased. The diagram of the Path Congestion Aware Adaptive Algorithm is given in fig.1.

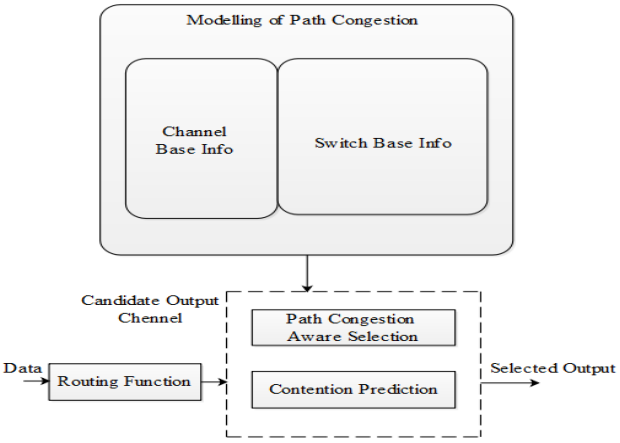

Fig. 1. Path Congestion Aware Adaptive Algorithm

Congestion aware arbiter algorithm consists of congestion aware selection function. This function works under two techniques. such as:

1. Congestion Aware Selection Strategy (CASS): This strategy is based on both channel congestion and switches the congestion information.
2. Congestion Prediction Techniques (CPT): This technique helps to change the capacity of buffer level from arbiter to next information state to determine whether congestion occurs in an adjacent paths or not.

A data stream is a sequence of digitally encoded signal that is used to transmit the data to a row buffer. A row buffer is considered as a data buffer used in the modern Dynamic Random Access Memory (DRAM) chips that allow quick and very simple access to the multiple data located in the physical row in the memory module. A memory bank includes several rows and columns of Storage Units (SUs) and is usually occupied in many chips. Only one bank can access the single read/write operation. Memory bank operation is controlled by Finite State Machines (FSM) which helps to design the sequential logic circuits. The data obtained from data stream is stored in buffer- in First - - First out (FIFO) manner. The overall block diagram of PCAR Router is given in fig. 2

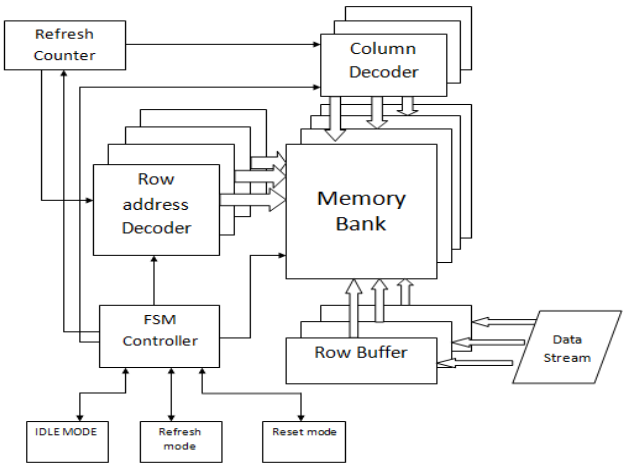

Fig. 2. Block Diagram of PCAR Router

FSM controller performs three operations namely write, idle mode and read mode. To perform the next operation, the refresh counter is used and the FSM is used to controls the read and write operation of FIFO. When FIFO is empty then the FSM controller performs write operation. When FIFO is full then the FSM controller performs read operation. Otherwise, the FSM controller is in the ideal mode. In this method, no-load bypass is used between memory and processor to increase the throughput. So, there is no need for storing the incoming bits in memory. When memory is empty, input bits are bypassed into the next stage which helps to reduce the latency. A priority-based arbiter approach will efficiently increase the throughput of the NoC architecture.

The priority selects the arbiter which has high favorable priority during the transmission process. With the help of the priority algorithm, the resources are allocated in NoC architecture. Then the latency of a given packet depends on the arbiter location. Arbiter with a low priority can preempt later.

B. Time Division Multiplier (TDM)

The course of events shared by switches is isolated into numerous openings having a fixed size. All the arbiters are required to be synchronized to space zero and know about the size of the pre-planned length. The TDM calculations must timetable all the arbiters, regardless of whether that doesn't have to transmit information. Henceforth, this procedure builds the idleness in arrange. To give a reaction time assurance to a multi-center locale with NoC, the correspondence delay requires to be upper limited. This examination investigates how TDMA attribution convention can be applied to NoC to deal with intermittent constant correspondence sets. TDMA is an intervention calculation, which directions access to a typical asset dependent on asset disengagement. This isolation is accomplished by isolating the entrance time to the common asset. Subsequently, the significant goal is to make a worldwide TDMA calculation to execute synchronously on all NoC components: organize interfaces and switches. The TDMA calculation licenses inference of the subsequent planning conduct for the multi-center framework, which utilizes NoC as its communication architecture.

The TDM based NoC establishes a subcategory of the circuit-switched NoC. In this research, a double-time wheeling method is used to facilitate a probe-based association setup in TDM NoC architecture. A path search algorithm is utilized in association setup that are no longer limited to deterministic arbiter algorithms with this TDM technique. Furthermore, the hardware cost can be easily minimized, since setup requests and data flows can coexist in a single network. Apart from the double-time wheeling method for connection setup, this paper also proposed a highway method that improves the slot utilization during data transfer. This method can accelerate the transfer of the data row while maintaining the linearity and Quality of Service (QoS).

C. Error prediction based on Viterbi algorithm

The error prediction process is the final step of this research work. Errors are predicted in the NoC structure by the Viterbi algorithm. The Viterbi algorithm is performed by forming the trellis structure, which is finally traced back to interpreting the received data. It minimizes the computational complexity by employing a simpler trellis structure. The Viterbi decoder is employed in several Forward Error Correction (FEC) applications where data is transmitted in systems and it is subject to errors before the reception. The Viterbi decoder has the property of compressing the bits of data input to half. Finally, 8:4 Viterbi decoder redundancy, delay, and computation time also minimized in the code.

IV. EXPERIMENTAL RESULTS

This section is explained by the experimental setup and result discussion of the LP- FTAA- NoC architecture. The performance of the proposed NoC architecture is evaluated in the Xilinx tool based on different devices. The architecture of the proposed arbiter is implemented utilizing Verilog language and simulation. Verilog is a Hardware Description Language (HDL) that is a textual setup used for defining electronic systems and circuits. Electronic design is applied in Verilog for verification through simulation, timing analysis, and logic synthesis.

Table- I: Path Congestion Aware Adaptive Algorithm

Device	Methodology	LUTs	Flip Flops	Slices	Frequency (MHz)
Virtex-4 xc4vfx 100	Existing [02]	2565/ 84352	4487/ 84352	3254/ 42176	523.002
	LP- FTAA- NoC	2256/ 84352	4256/ 84352	3072/ 42176	567.199
Virtex-5 xc5vfx 100t	Existing [02]	1568/ 64000	4659/ 64000	4582/ 64000	495.365
	LP- FTAA- NoC	1412/ 64000	4256/ 64000	4256/ 64000	528.765
Spartan 6-xc6slx100	Existing [02]	4996/ 63288	4393/ 126576	4658/ 126576	412.201
	LP- FTAA- NoC	4875/ 63288	4256/ 126576	4256/ 126576	458.29

Through the FPGA usage, LUT, flip-flop, slices, frequency and power are broke down and are a much reasonable stage for advanced channel plans.

The FPGA gives a configurable structure through a variety of customizable rationale modules, which are interrelated by programmable steering assets and encased by Input and output block (IOB). The NOC architecture is simulated and is verified using the Modelsim tool. Table.1 shows the results of an existing and LP- FTAA- NoC architecture. The proposed NoC design is suitable for Virtex 4- xc4vfx100, Virtex 5- xc5vfx100t and Spartan -6-xc6slx100. Three different types of adaptive arbitration schemes are used in proposed NoC architecture. Those results are tabulated above. The Virtex 5- xc5vfx100t is considered as a high configuration device, which provides better performance compared to Virtex-4 and Spartan 6. Figure 3 illustrates the comparison graph of a performance parameter of FPGA for adaptive arbitration methods, it is evident that the FPGA performances are reduced in the proposed NoC architectures design compared to the existing works.

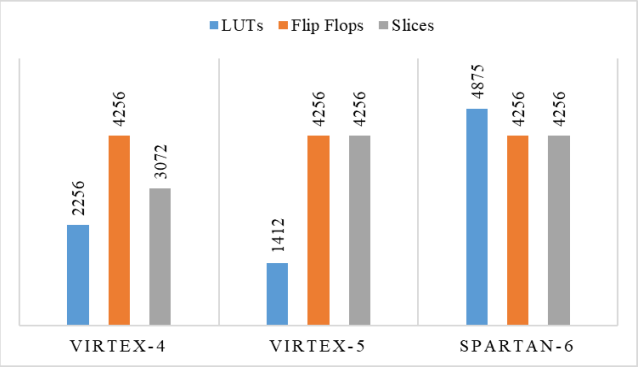

Fig. 3. Performance comparison graph for adaptive arbitration method

Table- II: comparison performance of the TDM with fault

Device	Methodology	LUTs	Flip Flops	Slices	Frequency (MHz)
Virtex -4 xc4vfx100	Existing [02]	3562/ 84352	42566/ 84352	5999/ 42176	245.325
	LP-FTAA-NoC	3159/ 84352	4174/ 84352	5966/ 42176	281.406
Virtex -5 xc5vfx100t	Existing [02]	3985/ 207360	4256/ 207360	4256/ 207360	412.701
	LP-FTAA-NoC	3836/ 207360	4096/ 207360	4096/ 207360	421.761
Spartan 6-xc6slx100	Existing [02]	4789/ 46648	4108/ 93296	42608/ 93296	203.209
	LP-FTAA-NoC	4682/ 46648	4008/ 93296	4008/ 93296	213.209

In table.2, the Adaptive Arbiter for 4x4 mesh topology NOC is implemented in the Xilinx tool and results are tabulated in this research. FPGA implementation is a much suitable platform for NoC architecture to evaluate the performances such as LUT, slice, flip-flop, frequency and Input-Output block (IOB). Analysing of Adaptive arbitration performance in Virtex-4 xc4vfx100, Virtex 5- xc5vfx100t and Spartan 6 – xc6slx100 are done in this research. The proposed Adaptive arbitration technique provides better performances in Virtex 4, Virtex 5 and the Spartan-6 FPGA when compared to the existing Fault-tolerant and Time-division based NOC architecture. The proposed system reduces 10 % of the LUT, 13% of the flip-flop and 20 % of the slices compared to the conventional methods in Spartan 6 devices. Also, this proposed pipelined NOC architecture operates at 281MHz, 421MHz and 213MHz in Virtex4, Virtex5 and Spartan6 devices respectively which shows that the proposed algorithm has a low delay and low power compared to existing approaches.

Fig. 4. The output waveform of the proposed NoC design

Figure.4 shows the FPGA output waveform of the complete NoC design using ModelSim, which validates the correctness of the design. The RTL schematic of proposed NoC architecture is shown in figure.5 which is taken from the Quartus II IDE tool by employing Verilog code. Each and every block contains a separate block which the as per the diagram.

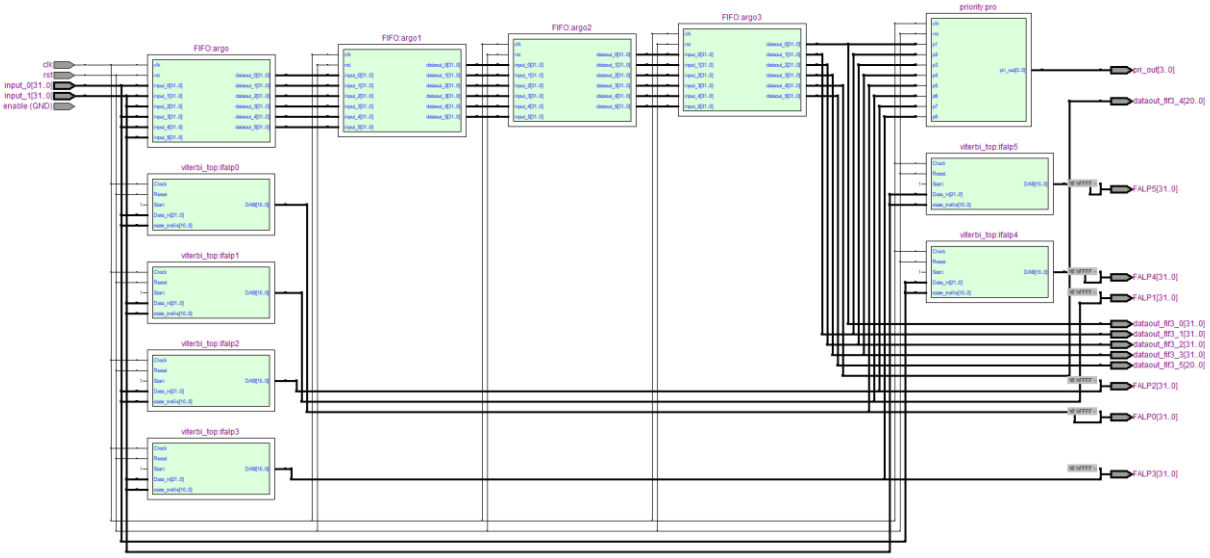

Fig. 5.RTL schematic of the proposed NoC architecture

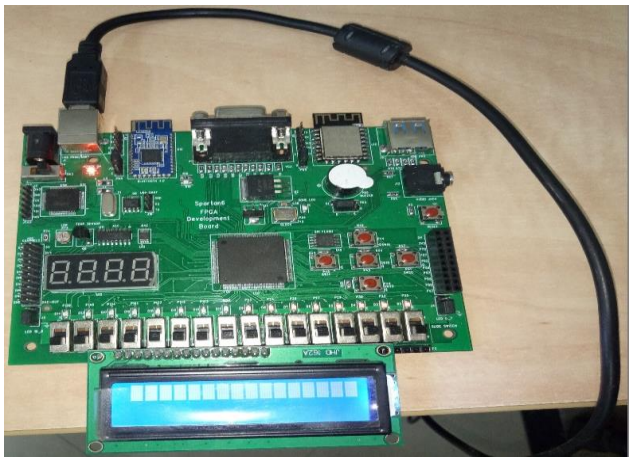

Fig. 6.Spartan 6 hardware setup

The hardware setup of the spartan 6 is shown in fig.6. The NoC architecture is implemented and the respective bit file is dumped in the spartan 6 hardware. With the help of UART cable, the system and spartan 6 hardware are connected to each other. With the HyperTerminal software, the information is sent to the FPGA. In FPGA, the NoC has performed the arbitration process to find the destination node. NoC prefers the less congestion path, high speed path, and less fault path to transmit the data to the designation. By using HyperTerminal software, the user can check the pathway of transmitting data. From this analysis, it is clear that the NoC arbitration is implemented in spartan 6 hardware perfectly.

V. CONCLUSION

In this research work, three different types of arbiter algorithms have been used, such as priority algorithm, TDM algorithm and Viterbi algorithm. All three algorithms were used to improve the linearity of the NOC. Initially, the priority algorithm helps to reduce traffic congestion when arbiter is in busy mode. Then, the fairness and QoS were maintained for proposed NoC architecture by the TDM algorithm. Finally, the Viterbi algorithm based error prediction process was applied in NoC architecture. Due to the usage of three proposed adaptive arbiter algorithms, the power consumption of the NoC was reduced. The packet can reach the destination using arbitration with less loss. Finally, FPGA performances of the proposed NoC were evaluated such as LUT, flip flop, slices, and frequency. The NoC architecture has implemented and is verified in Spartan 6 FPGA hardware. In the future, the area reduction mechanism will be implemented along with proposed arbitration to reduce the hardware utilization of the NoC architecture.

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