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Reduction of Test Time using Multiple Test Control Point Insertion for 7nm Technology Node

Maharshi Patel, Yogesh Parmar, Haresh Suthar

Abstract*: Test time reduction is a prominent challenge in scan based Design For Testability (DFT) architectures for cost effective test. Reliability and testability both are main objectives for DFT in today's VLSI design. In this paper, we have proposed multiple standard test control point insertion technique for 7nm technology node. The design was tested on 7828 sequential cells. We have compared results of following three Design Rule Check (DRC) (1) Scan DRC (2) Clock Scan DRC (3) Multiple standard test control point insertion DRC. We have used software tool Synopsys TetraMAX ATPG, Synopsys DFTMAX and Synopsys DFT compiler to verify the design. It has been observed that multiple standard test control point insertion DRC takes minimum time to check design of 7828 sequential cells.

***Keywords* : DRC, Scan insertion, DFT, VLSI.**

I. INTRODUCTION

As the complexity of VLSI circuits continues to increase, testing them economically becomes a challenging task. VLSI industries always bothered to find newer method to make design more reliable and testable. As the overall test-cost required to be reduce hence, testability of sequential/combinational circuits became tough task [1]. Tests based on scan architecture is the most predominantly used solution in order to achieve high fault coverage, the test doesn't consider the problems of large volume of test data which is recognized as one of major contributors to the test cost. Automatic test equipment (ATE) with high memory which can deal with increasing volume of test data is expensive [2]. Many compression schemes have been proposed to reduce the volume of test data needed to be stored in ATE by exploiting the don't care bits [3, 4, 5, 6]. Although a decompressed circuit should be designed to decompress the compressed data into original test patterns, test data compression can reduce the test data volume and test application time without degrading performance of the circuit[2].

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***** Correspondence Author
Maharshi Patel*, ECE, Parul University, Vadodara, Gujarat. India. Email: maharshipatel350@gmail.com
Yogesh Parmar, Assistant Professor, Department of Electronics and Communication Engineering, Parul Institute of Technology, Vadodara, Gujarat. India. Email: yogesh.parmar8031@paruluniversity.ac.in
Haresh Suthar, Assistant Professor & HOD, Department of Electronics and Communication Engineering at Parul Institute of Technology, Vadodara, Gujarat, India. Email: haresh.suthar@paruluniversity.ac.in

In order to put scan into the design, the design need to follow a set of scan design rules. Scan DRC is performed to repair design rule violations and allows the testable design to meet target fault coverage and it guarantees that the scan design will operate correctly. Advantage of performing the scan DRC is, it ensures the scan design by the different test protocols.

Scan DRC is initial step towards achieving higher fault coverage. But, it's always been time-taking taking process due to it checked that all cells in the design receiving signals with accuracy with timing, power, and without violation or with negligible violation. Scan design was previously implemented in [8] with linear feedback shift registers (LFSRs) in order to decompress the patterns into scan chains.

Clock scan DRC is to perform at-speed delay testing. Benefits of having clock scan DRC that clock controlling scan cells of the design are directly controllable from external pins. Additional care must be taken in terms of the way the clocks are applied in order to guarantee the success of the shift/capture operation. This mainly due to the clock skew between different clock domains is typically large. A data path originating in one clock domain and terminating in another might result in a mismatch [9].

To reconfigure the scan chains in our design to suit various tester requirements by defining different modes of operation, called test modes. Each test mode is activated by asserting one or more test-mode signals according to a particular test-mode encoding. Different test modes can have different scan-in and scan-out pin counts, and can even have independent sets of scan-in and scan-out pins altogether. The advantage of multiple test point insertion allow scan chain to bifurcate the test patterns in needed area. i.e., if scan cell no.1 to scan cell no.75 from scan chain 1 and scan cell no.12 to scan cell no.25 of scan chain 2 require same test vectors then, test point bypasses the path after scan cell no.75 of scan chain 1 to scan cell no.12 of scan chain 2 [10,11].

The paper is organized as under: the section –II discusses on the results of scan DRC, section –III discusses on results of clock SCAN DRC, section –IV discusses on results of Multiple standard test control point insertion DRC, section-V ends with conclusion. References are given at the end of paper.

II. RESULT OF SCAN DRC

Consider an example of a D flip-flop before and after scan substitution using the multiplexed flip-flop scan style shown in the Fig.1. The pin connection mappings are shown in parentheses.

In this example, the scan-in pin is SI, the scan-enable pin is SE, and the scan-out pin is shared with the functional output pin Q.

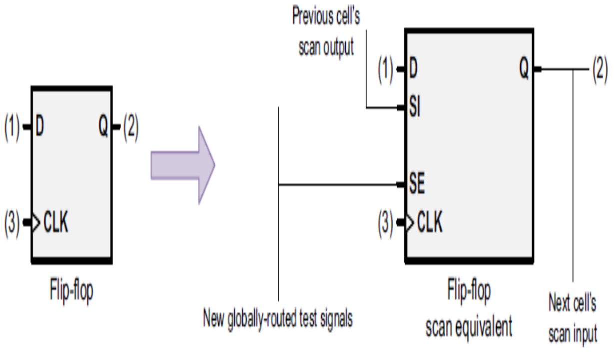

Fig. 1. D Flip-Flop After Multiplexed Scan Cell Substitution

From Fig. 1, it is understood that by adding Multiplexer pins into D flip-flop we can make scan flip-flop.

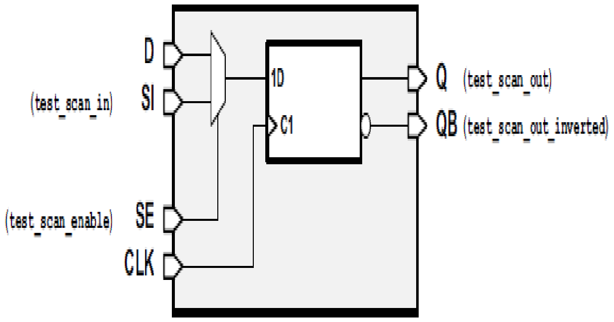

Fig. 2. Default Multiplexed flip-flop scan cell

Fig. 2. shows the default multiplexed flip-flop made by DFTMAX tool. Here pin connections are as SI_ScanDataIn, SE_ScanEnable, Q_ScanDataOut and QB_ScanDataOUT. By following these, scan design of total 7828 scan equivalent flip-flops is generated. Total 7828 Scan flip-flops are distributed in into 8 scan chains. By Applying scan_enable obtained output from scan_out pin as shown in following Fig. 3.:

ELAPSED TIME	AREA	WORST NEG SLACK	TOTAL SETUP COST	DESIGN RULE COST
0:01:19	82487.6	0.00	0.0	0.3
0:01:19	82487.6	0.00	0.0	0.3
0:01:25	82475.3	0.00	0.0	0.3
0:01:26	82465.4	0.00	0.0	0.3
0:01:27	82460.2	0.00	0.0	0.3
0:01:27	82459.2	0.00	0.0	0.3
0:01:27	82458.5	0.00	0.0	0.3
0:01:27	82458.5	0.00	0.0	0.3
0:01:27	82458.5	0.00	0.0	0.3
0:01:27	82458.5	0.00	0.0	0.3
0:01:27	82458.5	0.00	0.0	0.3
0:01:27	82458.5	0.00	0.0	0.3
0:01:27	82458.5	0.00	0.0	0.3
0:01:27	82458.5	0.00	0.0	0.3
0:17:59				4.2

Fig. 3. Scan DRC Result

From Fig. 3, it is observed that by completing the scan operation it takes 17:59 nanoseconds and the total cost to run the scan DRC is 4.2 $ US dollar, which is highlighted in above Fig. 3.

III. RESULT OF CLOCKED SCAN DRC

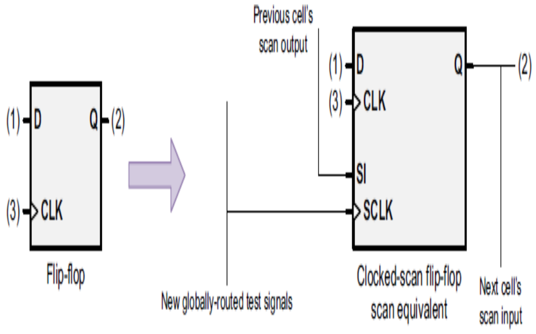

Fig. 4. D Flip-Flop After Clocked-Scan Cell Substitution

The clocked-scan scan style uses a separate dedicated edge-triggered test clock to provide scan shift capability. In functional mode, the system clock is active and system data is clocked into the cell. During scan shift, the test clock is active and scan data is clocked into the cell.

Fig. 4. shows an example of a D flip-flop before and after scan substitution with the clocked-scan scan style. The pin connection mappings are shown in parentheses. In this example, the scan-in pin is SI, the dedicated edge-triggered test clock pin is SCLK, and the scan-out pin is shared with the functional output pin Q.

In this test pins connections the test_cell group of the scan cell description in the logic library, are required on a clocked-scan cell: Scan-input, Test-clock and Scan-output (can be shared with a functional output pin).

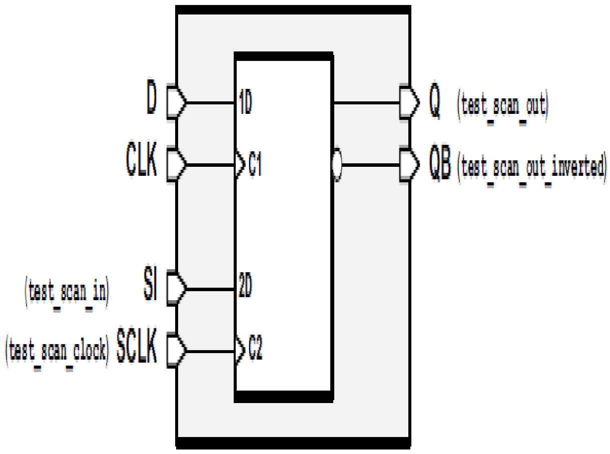

Fig. 5. Default clocked-scan flip-flop scan cell

Above Fig.5 shows the default clocked-scan flip-flop scan cell generated by DFTMAX tool. The pin connections identifies as: SI_ScanDataIn, SCLK_ScanMasterClock, Q_ScanDataOut, QB_ScanDataOut. By following these default clocked-scan style scan flip-flops, again we set total 8 scan chains for total 7828 flip-flops. We get result as follows:

ELAPSED TIME	AREA	WORST NEG SLACK	TOTAL SETUP COST	DESIGN RULE COST
0:00:47	90691.2	0.00	0.0	38.5
0:00:47	90691.2	0.00	0.0	38.5
0:00:48	95653.9	0.00	0.0	2.5
0:00:50	95653.9	0.00	0.0	2.5
0:00:50	95653.9	0.00	0.0	2.5
0:00:50	95653.9	0.00	0.0	2.5
0:00:51	95653.9	0.00	0.0	2.5
0:01:04	82419.4	0.00	0.0	2.4
0:01:05	82418.2	0.00	0.0	2.4
0:01:13	82418.2	0.00	0.0	0.9
0:01:13	82418.2	0.00	0.0	0.9
0:01:14	82418.2	0.00	0.0	0.9
0:01:14	82411.1	0.00	0.0	0.9
0:01:14	82411.1	0.00	0.0	0.9
0:01:14	82411.1	0.00	0.0	0.9
0:01:14	82411.1	0.00	0.0	0.9
0:01:14	82411.1	0.00	0.0	0.9
0:14:62				101.5

Fig. 6. Scan Result with Additional Clock (Clock DRC)

By Fig. 6, we can show that the total elapsed time of clocked scan DRC is 14.62 nanoseconds and cost is reached to 101.5 $ which is highlighted in above Fig. 6.

IV. RESULT OF MULTIPLE TEST CONTROL POINT DRC

After having much more complexions in scan run and clocked-scan run. We need a technique that can separate the complex scan environment and make it simple reliable and testable environment. So, first we decide a scan chain which has no violations or very less no. of violations. Then, we insert control point to the scan chain to control the path of test patterns. Same way we apply this for all remaining scan chains. No. of control point per scan chain is may be or may be not directly depends on the no. of affected nets and scan cells. Well, this approach of testing is not mandatorily use for every time. But, it is applied when critical testing (when various testing perform on same time to observe every single response of chip) need to perform. Insertion of control point became possible DFTMAX tool, the simple idea of adding control_01 is as follows as per Fig.7.:

The control_01 test point requires two scan cells per control point, one for the source signal value and one for the enable register that specifies that the source signal should be driven. A control_01 test point is similar to the control_0 and control_1 test point types. The early idea of test point insertion taken from [12] and through this approach we get idea of how to perform with multiple test mode.

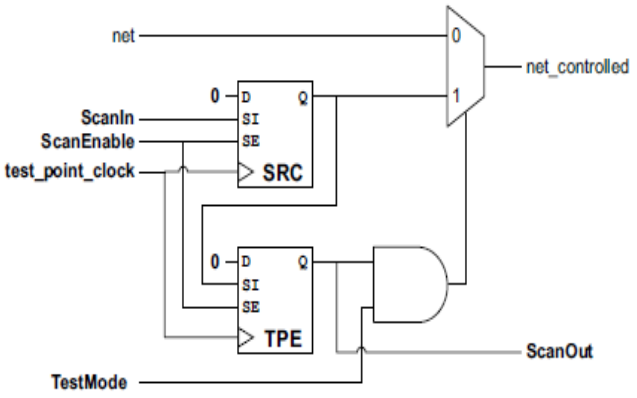

Fig. 7. Example of control_01 test point

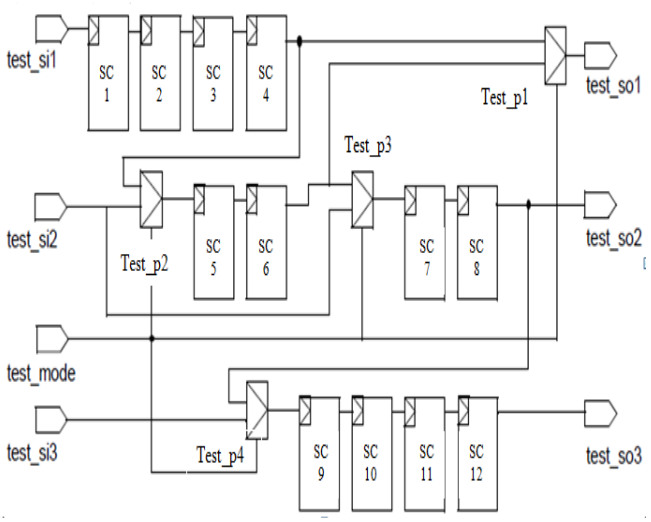

Fig. 8. Scan Structure with Multiple Test Control Point Insertion

Here, example below having a simple design with 12 scan cells that must operate in two different scan modes. In one mode, scan data is shifted through two chains (six cells each), and in the other mode, scan data is shifted through three chains (four cells each).

ELAPSED TIME	AREA	WORST NEG SLACK	TOTAL SETUP COST	DESIGN RULE COST
0:00:14	84357.1	0.00	0.0	7.7
0:00:14	84358.1	0.00	0.0	7.1
0:00:14	84359.1	0.00	0.0	6.5
0:00:14	84360.1	0.00	0.0	5.8
0:00:14	84361.1	0.00	0.0	5.2
0:00:14	84362.1	0.00	0.0	4.6
0:00:14	84363.1	0.00	0.0	4.0
0:00:14	84364.1	0.00	0.0	3.4
0:00:14	84365.1	0.00	0.0	2.8
0:00:14	84366.1	0.00	0.0	2.2
0:00:14	84367.2	0.00	0.0	1.6
0:00:14	84368.2	0.00	0.0	1.0
0:00:14	84369.2	0.00	0.0	0.4
0:00:14	84370.0	0.00	0.0	0.0
01:96				52.3

Fig. 9. Scan result with TCPI

V. EXPERIMENT RESULT

Experiment done on the design having 8 scan chain, and total 7828 scan cells.

Table- I: EXPERIMENT RESULT

Sr. No	Type of DRC	Seq. Cells	Violated Seq. Cells	Valid Cells	Valid Cores	Scan Chain	Elapsed Time During DRC in nanosecond
1	Scan DRC	7828	159	7669	24	8	17.59
2	Clock Scan DRC	7828	205	7623	24	8	14.62
3	Multiple standard test control point insertion DRC.	7828	159	7669	24	8	1.96

VI. CONCLUSION

The design of 7828 sequential cells of 7nm technology node was tested using following three Design Rule Check (DRC) (1) Scan DRC (2) Clock Scan DRC (3) Multiple standard test control point insertion DRC. The results obtained for all three methods are shown in Table-I. From the results, it is concluded that Scan type DRC has violated sequential cells 159, valid cells 7669, valid cores 24, scan chain 08, and elapsed time during DRC 17.59 nanosecond. Clock Scan DRC has violated sequential cells 205, valid cells 7623, valid cores 24, scan chain 08, and elapsed time during DRC 14.62 nanosecond. Multiple standard test control point insertion DRC has violated sequential cells 159, valid cells 7669, valid cores 24, scan chain 08, and elapsed time during DRC 1.96 nanosecond.

The minimum value of violated sequential cells 159 obtained in both Scan type DRC and Multiple standard test control point insertion DRC. The minimum value of elapsed time during DRC is 1.96 obtained in Multiple standard test control point insertion DRC. Hence, it is concluded that Multiple standard test control point insertion DRC outperformed compared to other two DRC methods.

REFERENCES

1. Binod Kumar, Boda Nehru, Brajesh Pandey and Jaynarayan Tudu; Skip-scan: A methodology for test time reduction; 2016 IEEE.
2. Hyeonchan Lim, SungyoulSeo, Soyeon Kang and Sungho Kang; “Broadcast Scan Compression based on deterministic pattern generation algorithm; 2017 IEEE.
3. Touba, Nur A; “Survey of test vectors compression techniques”IEEE Design & Test of Computers, 2006, vol. 23, no.4,pp.294-303.
4. Bayraktaroglu, Ismet, and Alex Orailogl;, "Decompression hardware determination for test volume and time reduction through unified test pattern compaction and compression," VLSI Test Symposium, Proceedings. 21st. IEEE, 2003, pp. 113-118.
5. Krishna C. V., Touba Nur A; “Reducing test data volume using LFSR reseeding with seed compression,” Test Conference Proceedings. International. IEEE, 2002, pp. 321-330.
6. Tenentes V., Kavousianos K., and Kalligeros E; "Single and variable-state-skip LFSRs: bridging the gap between test data compression and test set embedding for IP cores," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, vol. 29, no. 10, pp. 1640-1644.
7. Laung-Terngwang, Cheng-Wen Wu, Xiaoqing wen, a book on VLSI Test Principles and Architecture, 2006 edition.
8. Acevedo, Oscar, and Dimitri Kagaris; Computation of LFSR characteristic polynomials for built-in deterministic test pattern generation; 2016 IEEE.
9. J. Balcrek, P.Fier, and J. Schmidt; On don’t cares in test compression; Microprocessors and Microsystems 2014.
10. Ms. Janki Chauhan, Mr. Chintan Panchal, Prof. Haresh Suthar; Scan Methodology and ATPG DFT technique at Lower Technology Node; IEEE 2017.
11. Mr. Maharshi Patel, Mr. Yogesh Parmar, Mr.Chintan Panchal; An Analysis on Various Implemented Scan Insertion Technique that Reduces the Test Application Time; IJTIMES 2019.
12. Priyanka N. Solanki, Nilesh Ranpura and Yogesh D. Parmar; DFT Methodologies for Reducing Shift Power of Compression Architecture for 28nm ASIC; ICOEI by IEEE 2018.

AUTHORS PROFILE

Maharshi Patel, is a student of M. Tech from Vlsi Design and Embedded System Engineering, from Parul University. This result was obtained during his industrial training. As a member of DFT team, he finishes his internship of duration 1 year.

Yogesh Parmar, is working as Assistant Professor in a Department of Electronics and Communication Engineering, Parul Institute of Technology, Vadodara, Gujarat. His main focus area of research is ASIC Design. He has 8 Years of teaching experiences and more than 20 publications in refereed international journals and conferences.

Haresh Suthar is working as Assistant Professor & HOD in a Department of Electronics and Communication Engineering at Parul Institute of Technology, Vadodara, Gujarat, India. He has 10 Years of teaching experiences..