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Architecture of 2X2 FIR Filter using Vedic Multiplier and Brent-Kung Adder

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Abstract: ***This paper proposed, a 2X2 FIR filter which is based on the Brent-Kung adder and Vedic multiplier. A 2X2 FIR filter has been designed using Brent-Kung-Adder (BKA) and filter coefficient. Verilog platform and Xilinx 14.5 software. The Brent-Kung adder is much faster than the look ahead carry adder (LACD), carry select adder and ripple carry adder (RCA) and it is a parallel prefix adder. Lowarea and the power consumption in Brent-kung adder is also less as compared to various adders. Multiplication of a number using the Vedic multiplier is arithmetic key operation to be performed with low power consumption of and increase the speed in the consequence applications. Proposed design utilize the common multiplication in cross multiply to compensate the problem of delay which is occurring in the Booth Multiplier and Array Multiplier and etc. Brent-kung adder used to decrease the delay which was occur in the multiplier and significantly reduce the quantity of logic elements such as gates, signals etc.***

Key words: Brent-kung Adder, FIR Filter, Delay, Parallel prefix adder, Vedic multiplier.

I. INTRODUCTION

The FIR filter is used in various applications, such as video processing, wireless communications, image processing, etc. An FIR filter is a filter structure in which multipliers are fundamental to develop the computationally vigorous DSP entities like MAC, DFT (Multiply Accumulate, Discrete Fourier Transform). Any processor speed is depends upon the multipliers [1], [2]. Hence to design, the parallel and reconfigurable Field programmable Gate Array (FPGA) have its origin in hardware architecture are needed. In broad band area of wireless communication approaches a major importance is received in the complex multiplication process, because of wireless channel complex nature. To implement the hardware modules a great number of compound multipliers are necessary [3]. A multiplier has designed originate from on Vedic multiplier that the vedic multiplier is much faster than the Array multiplier. The adders are very important in digital circuits. The processors and systems speed can be improve by increase in the speed of the adders and multipliers that result minimum delay. In now a days in digital signal processing, multipliers plays an important role and in various other applications. Serial adders are used where are power and area are of maximum value and high delay can be tolerated. In a faster version of the iterative multiplier, partial products should add at once.

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FIR filter: FIR filter is also known as recursive filter. The factual meaning of the recursive is running back and technically refers, the previously calculated outcomes are going to be the new outputs[4]. For processing, filtering operations in the every stage of the FIR filter the previous output values are uses with addition of input values. Hence it is known is recursive filter.
So from the above discussion, it is clear that more calculation is needed to perform the FIR filter process, since the filter expression consist both terms, i.e. previous output terms and present input terms. The output of Finite Impulse Response filter is represented in Punskaya (2005) as,

$$Y(n) = \sum_{k=-M_1}^{M_2} b_k \; X(n-k) \qquad (1)$$

Here, the variables M_1 and M_2 are finite.
In one of the more simple FIR filter, here itcan be considerable thatthe form- 3 term moving average filter as shown in **Figure 1**,

$$Y(n) = \frac{1}{3}[X(n-1) + X(n) + X(n+1)] \qquad (2)$$

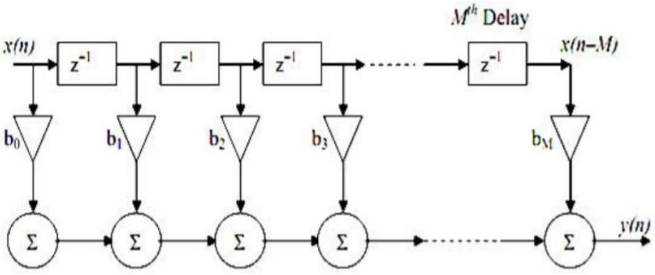

Figure 1: Direct Form FIR filter

II. LITRATURE REVIEW

G. Challa Ram et.al, they approach the delay comparison of Wallace multiplier with dadda and array multiplier. Further an implementation is proposed on 16 bit Wallace multiplier via binary to excess-1 convertor (BEC) and carry select adder (CSLA). They get less delay when using CSLA as compared to Wallace multiplier with BEC. In the paper proposed by them the code simulation and synthesization is done by XILINX software 12.2 on spartan 3E FPGA device xz3s500-5fg320 [1][16].

In the work proposed by Dravik KishorBhai Kahar et.al, he has developed less time delay and less slice used in vedic mathematics. In the proposed paper the number of slices used in vedic multiplier is 403 for 16X16 bit, while other multipliers use 412 slices. As the slices are reduced the time delay automatically reduced and area is also reduced in this proposed paper[5] [12].

K. Deergha Rao et.al, they proposed theVedic real multiplier design which is originate from Urdhva Tiryakbhyam sutra,which is a part of the ancient Indian Vedic Mathematics. They discover the analysis of path delay of two achievable architectures are, i) four Vedic real multipliers solution, ii) three Vedic real multipliers solutionhas performed.
And to develop an expression for minimum path delay architecture of the vedic real multiplier for N bit. It is also seems that the minimum when it compares with other multiplier or booth multiplier, but it is seen that the power consume by the vedic complex multiplier is greater than the array multiplier[6] [13] [14].
Ranjan Kumar Barik et.al, they proposed a multiplier less technique for the smaller area, which was originate from the add and shift technique & common sub-expression elimination. Which is also reduced the power and increase in speed implementations of FIR filters.That design performed much quicker than the MAC filters, but this design used the embedded multipliers using of FPGA devices [7] [12] [15].
In the work proposed by L kholee phimu et.al, they have observed that by replacing binary subtractor via carry look-ahead subtractor and binary adder by a carry look-ahead adder and multiplier with booth multiplier in an area-efficient 2 parallel FIR filter, the delay and area were improved.Area and speed of area -efficient 2-parallel FIR filter have a better performance then proposed 2-parallel FIR filter. The simulation was done on Xilinx ISE 14.2 ISE to observe the output waveform and the simulation and implementation was carried out in IMAGE system to authenticate the output obtained from the FPGA[1][8] .
In the work proposed by Pushpalata Verma, she found 4X4 bit vedic multiplier based on "Urdhava Triyakbhyam" sutra. The design was implemented on the Spartan xc3s50a-5-tq144 device of 4X4 bit vedic multiplier. The computational path delay of multiplier is found to be 13.102 ns. When it compared to conventional multipliers it seems highly efficient in the terms of the speed [9][10].

III. METHODOLOGY[11]

A. Vedic Multiplier

The multiplier which is originated from the Vedic Mathematics is a of type of small power and fast speed multiplier. Employeing this techniqe in the multiplication computation algorithms will be redude the program execution time, complexity etc.The vedic multiplier system is based on the 16 Vedic Sutras, which describes the natural ways of solving a whole range of mathematical troubles. Out of these 16 Vedic Sutras the Urdhva-Triyakbhyam surta is commonly used multiplication formula, which is applicable for all the cases. It litrally means vertically and crosswise.
Considered two B-bit operands $x_{B-1}, x_{B-2},\ldots x_2, x_1, x_0$ and y_{B-1} $y_{B-2}\ldots y_2\ y_1\ y_0$ for B by B multiplier.

Vedic Multiplier Method: - Let X and Y areb-bits numbers such that multiplication of the inputs X and Y gives the 2b bits product. Here X and Y are split into two partsas X_0, X_1 and Y_0, Y_1 each consisting of b/2 bits. X and Y be expressed as

$$X_0 = X(\frac{b}{2} - 1\ to\ 0) \quad (3)$$

$$X_1 = X(b-1\ to\ \frac{b}{2}) \quad (4)$$

$$Y_0 = Y(\frac{b}{2} - 1\ to\ 0) \quad (5)$$

$$Y_1 = Y(b-1\ to\ \frac{b}{2}) \quad (6)$$

i) URDHVA-TRIYAKBHYAM SUTRA: Consider two binary numbers a1a0 and b1b0. Both binary numbers have 2 bit volumn, in which a1a0 is multiplicand and b1b0 is multiplier.
1)In the final product, to obtained the lowest significant bit s0 the multiplication is done vertically between multiplicand and multiplier of the lowest significant bits (LSBs)as shown in Figure 2.

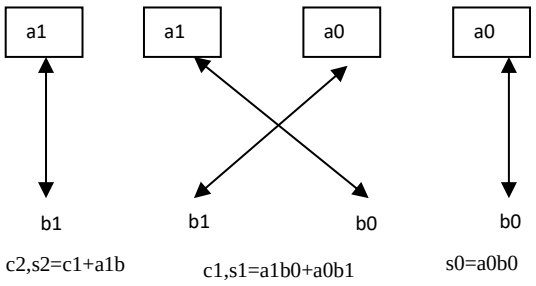

Figure 2: Urdhya Triyagbhyam method

2) To achieve the second bit s1 to the final product and the carry bit c1, the addition of the two product term (a1, b0 and a0,b1) is done, which is originate from Urdhava Triyakbhyam" sutra which simply mean vertically and crosswise as shown in Fig. 2.

3) And in the end to achiev the third bit s2 ant the carry c2 to the final product vertically multiplication is done between the a1 and a0 MSBs

ii)**2 x 2 BIT VEDIC MULTIPLIER:** Two cross two Vedic multiplier can be implemented using four two input AND gates and two half adders as shown in Figure 3. 2X2 bit Vedic multiplier works on the process as discussed above.

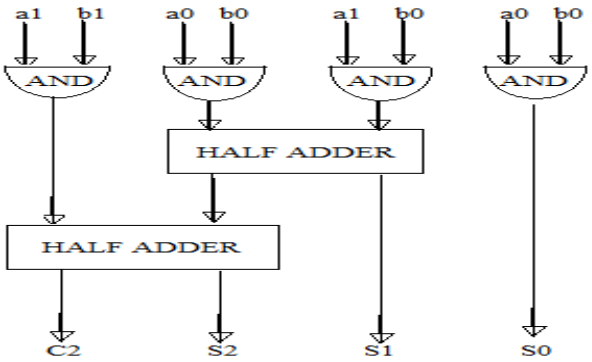

Figure 3 : Block Dig. Of 2X2 Vedic Multiplier

iii) 4X4 BIT VEDIC MULTIPLIER: Let the two binary no. a3 a2 a1 a0 and b3 b2 b1 b0.

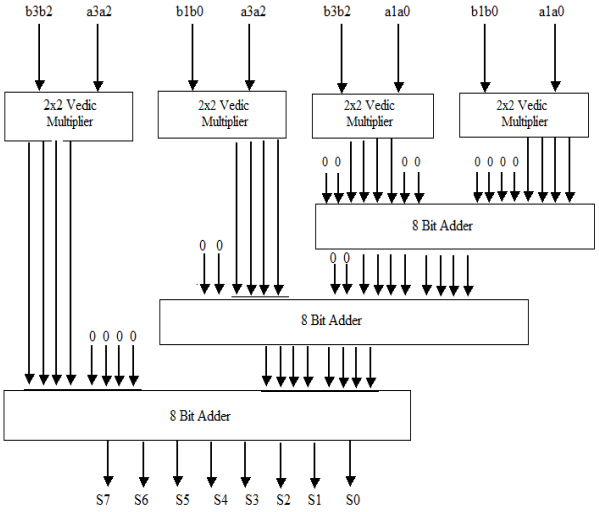

Figure 4 : An architecture of 4X4 bit Vedic Multiplier

Divide the multiplier into two parts each considering of two bits as b3b2 and b1b0. In the same way divide the multiplicand into two parts as a3a2 and a1a0. It usually use the 2X2 bit vedic multiplier and taking two binary bits at a time and using 2X2 bit Vedic Multiplier the possible architechture four cross four bit vedic multiolier as shown in figure 4 the final product of multiplier is S7, S6, %, S5,S4, S3, S2, S1, and S0. The figure shows the architechture of 4X4 bit vedic multillier which contains four 2X2 vedic multiplier and three 8 bit adders.

B. Brent Kung Adder

The Brent–Kung adder is a parallel prefix adder (PPA) and it is modified form of CLA (Carry look ahead adder). It is faster the different types of adders like, ripple carry adder (RCA), carry look ahead adder (CLA), etc. This adder has less wiring issues, reduced the complexity and it is less area and power consuming adder. Architecture of Brent-kung adder is shown in Figure 5.

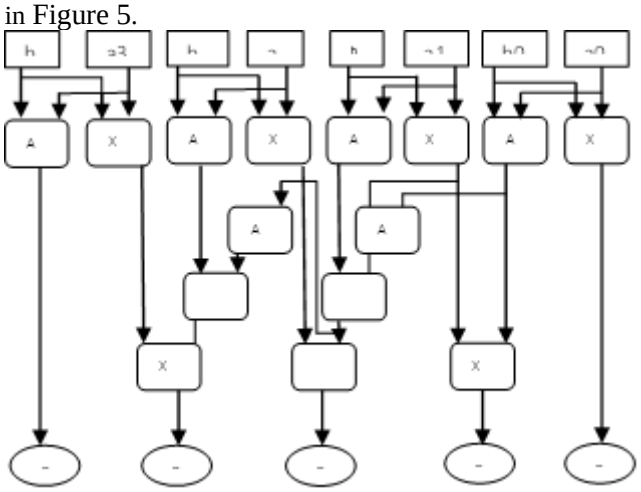

Figure 5: Block Diagram of Brent Kung Adder

IV. SIMULATION RESULT AND ANALYSIS

In this proposed paper the the Xilinx 14.5i updated version is used to design and experiment the algorithm. (Xilinx 14.2i has combination of the significant features justfast debugging small memory necessity and small price. The less memory necessity approximate 27 percentage less provided by the newesstliberate of ISE™ (Integrated Software Envirosnment) designing tool gives. The advanced tool is provided by the 14.5i as smart compile technology in its result it shows more faster time closer and good usage of their computing hardware, for a better timing to design solution. ISE 14.5i Xilinx tools authorizesmoreworkability for the designs which grip embedded processors. The ISE 14.5i Design train is conduct by the librate of chip scope Pro™ 14.5i debugging and verification of the software. We can debugthe program smoothly by the use of that software. It is alsoenvolved its current librate of the chip scope Pro Serial IO Tool kit, which is giving simplified debugging of more speed serial IO designs for the Virtex-5 LXT and also for the Virtex-4 FX and and SXT Field Programmable Gate Arrays. With the aid of this advanced tool we can succeed in the communication area as well as in the signal processing area and VLSI low power designing.

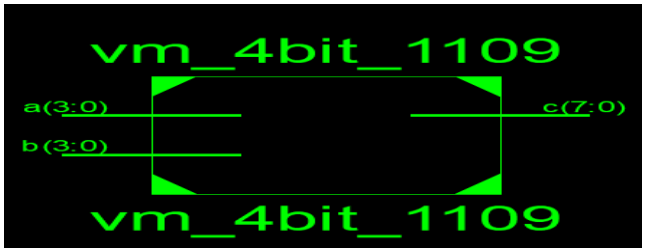

Figure 6: View Technology Schematic of 4X4 Vedic Multiplier.

View technology schematic of 4X4 bit Vedic multiplier is shown in Figure 6 which has two 4-bit input “a” and “b” and an8-bit output “c”. When two binary number will be multiplied then the number of output bits of the multiplier will be addition of the bit of both input.

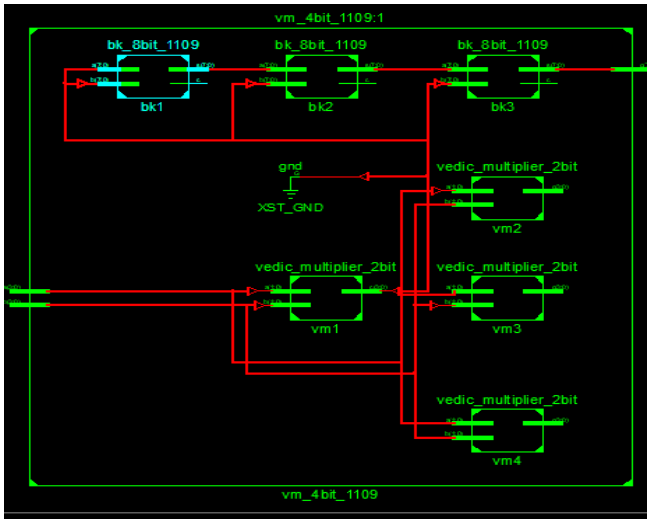

Figure 7: RTL View of Vedic Multiplier

In the Figure 7shows the RTL view of 4X4 Vedic multiplier which is made by 4 numbers of 2X2 multiplier and 3 numbers of 8-bit Brent-kung adder.

```
Timing Summary:
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Speed Grade: -5

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 9.452ns

--------------------------------------------------------------------
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Figure 8: Timing Summary of 4X4 Vedic Multiplier

Figure 8shows the timing summary of the 4X4 bit Vedic multiplier which is shows that the maximum combinational path delay of 4X4 Vedic multiplier is 9.452ns and no any clock used in this method so no any path shown for the clock and also not used any timing control.

vm_4bit_1109 Project Status			
Project File:	vedic_multiplier_1.xise	Parser Errors:	No Errors
Module Name:	vm_4bit_1109	Implementation State:	Synthesized
Target Device:	xc3s1600e-5fg320	• Errors:	No Errors
Product Version:	ISE 14.5	• Warnings:	No Warnings
Design Goal:	Balanced	• Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	
Environment:	System Settings	• Final Timing Score:	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	15	14752	0%
Number of 4 input LUTs	27	29504	0%
Number of bonded IOBs	16	250	6%

Figure 9: Device Utilization summary of 4X4 Vedic Multiplier

Device utilization summary shown in Figure 9 which is shows that LUTs Number, Number of slices and the number of IOBs used in the 4X4 Vedic multiplier is 15, 27 and 16 respectively.

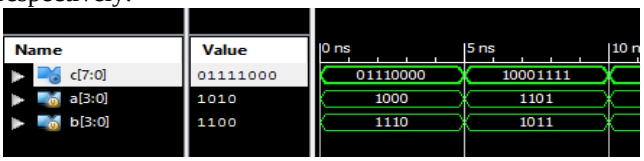

Figure 10: Verilog Test Bench of 4X4 Vedic Multiplier

Test bench simulation of 4X4 Vedic multiplier is shown inFigure 10. Here shows that when taking two 4-bit binary input a[3:0] is 1000 and b[3:0] is 1110 then the 8-bit output c[7:0] is 01110000 and input a[3:0] is 1101 and b[3:0] is 1011 then the 8-bit output c[7:0] is 10001111.

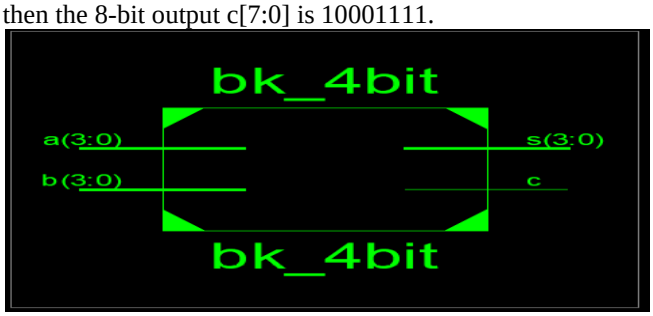

Figure 11: VTS for 4-bit BK Adder

Figure 11 shows the view technology schematic of 4-bit brent kung adder which has two 4-bit input "a", "b" and a 4-bit output sum is "s" and an another output carry is "c".

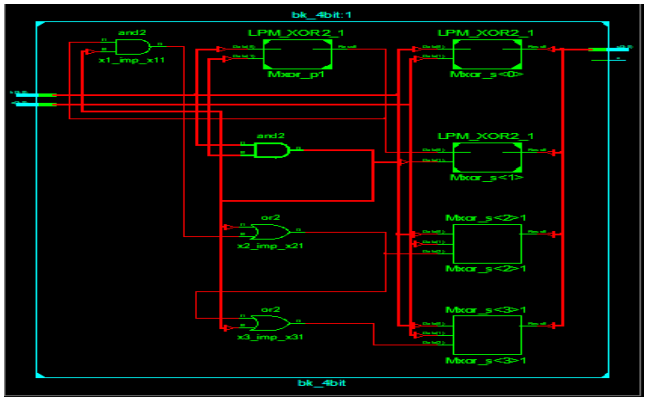

Figure 12: RTL View of 4-bit BK Adder

Shows the RTL view of Brent-kung adder in Figure 12which has total 43 gate court is used.

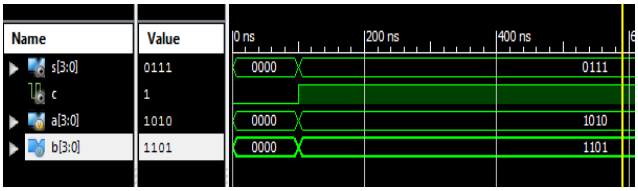

Figure 13: Verilog Test Bench of 4-bit BK Adder

In the Figure 13shows the test bench simulation of 4-bit Brent Kung adder in which when two input "a" is 0000 and b is 0000 then output sum "s" is 0000 and output carry "c" is also 0. When input "a" is 1010 and "b" is 1101 then the output sum "s" is 0111 and carry "c" is 1.

Table 1: Delay comparison Result of Previous Multiplier and Proposed Multiplier

Multiplier Bit	Previous Method	Proposed Method
4X4	11.477ns	9.452ns
8X8	21.550ns	12.981ns
16X16	28.086ns	16.660ns
32X32	30.956ns	20.527ns

The delay comparison result of previous multiplier and proposed multiplier is shown in table I in the form of multiplier bits in the proposed method and proposed method.

Table 2: Area comparison result of previous multiplier and proposed multiplier.

Multiplier Bit	Number of slices utilized in previous method	Number of slices utilized in proposed method	Number of LUTs in Previous method	Number of LUTs in Previous method
4X4	18	15	31	27
8X8	91	69	159	122
16X16	403	324	710	567
32X32	1639	1369	2900	2391

Area comparison result of previous multiplier and proposed multiplier in the term of difference mathods is show in the Table 2.

V. CONCLUSION

In previous design, ripple carry adder was used for designing parallel FIR filter but it was having the drawback that it was not working for every bit and large circuit complexity. So to remove this drawback, Brent Kung adder has used which is an advanced binary adder. It reduces the cost and the complexities of wire and more over, it is much quicker than Ripple Carry adder and carry look ahead adder. Hence provides better performance and less area to implement in comparison to Kogge Stone adder. Further advantage of using Brent Kung adder is that it works on every bit and consumes less space.

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