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Programmable FFT Processor using Dual RAM and ROM Technologies for Future 5G Communications

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Abstract : The high-throughput programmable Fast Fourier transform processor supports the usage of 2-stream 1024/2048/4096-point Fast Fourier Transforms and 1-to 4-stream 64/128-point Fast Fourier Transform for 4G,wireless local networks and for 5G.The proposed architecture which was designed is a well-intentionedfour-bank single-port SRAM which is being working in four-word data width, the design which is proposed gives us sixteen memory pathways . where the data is accessed up to this extent where it can be used in upcoming 5G. The radix-16 butterfly process element comprises of 2 cascaded parallel, pipelined radix-4 butterfly units which is specified. The projected memory-addressing methodology will effectively wear down single-port, merged-bank memory with high-radix process components. Comparing with typical memory based Fast Fourier Transform styles, the derived design has higher performance in expressions of area and power consumption. The architecture which is projected occupies the tiniest area of around1.21mm^2.The processor supports 1966MS/s 4096-point FFT and frequency of 1GHz.The Electronic design automation synthesis results show the power consumption is 32.16mW.The SQNR performance analysis is 42.14 dB.

Index-Terms: Discrete Fourier Transform(DFT), Fast Fourier Transform(FFT), Electronic design automation(EDA) Orthogonal frequency division multiplexing(OFDM).

I.INTRODUCTION

Fast Fourier Transform is an algorithm which figures discrete Fourier Transform of a grouping sequence, or its inverse (IDFT).Fast Fourier transform domain in digital signal processing is an operative tool for a range improvement of spectrum enrichment of orthogonal frequency division multiplexing primarily based waveforms, that may be acentral element within the fifth generation of recent radio developments.FFT processor is one amongst the key elements surrounded by the accomplishment of wideband of OFDM systems[1].Architectures having structured Pipeline need'sto meet up the fast, real-time processing low-power utilization pre-requisite within an exceedingly portable environment. OFDM is employed in an exceedingly massive vary of applications from weird-communication modems[2][3] like digital subscriber lines[5] to wireless communiqué modems, like WiMAX or the 3GPP long-term evolution(LTE), for processing of baseband data.

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The Fourier transform which is utilized to convert the signals from time domain to frequency domain and alsosimilarly the inverse Fourier Transform is employed to adapt the signal back from the frequency domain to the time domain[1]. The Fourier transform may be a powerful tool to evaluate or to research the signals and construct them both the to and from of their frequency components. The signal which is discrete in time that is sampled and solitary use the discrete Fourier transform to convert them into the discrete frequency form DFT and vice-versa of it, the inverse discrete transform is employed to back convert the discrete frequency structure into the discrete-time form. In Transmitters exploitation OFDM as a multicarrier modulation technology, the OFDM symbol is made within the frequency domain by mapping the giveninput bits on the 2 components that is I and O parts(components) of the QAM symbols and then ordering them in an exceedingly sequences with a sequence with a selected length in step with the amount of subcarriers within the OFDM symbol[4].this method is done by the ordering and mapping which constructs the frequency components of the ofdm symbol. To transmit them, the signal must be symbolized in time domain and this is consummate by the inverse FFT. Many OFDM systems like 4G LTE and wireless local area networks, need non-power two discrete Fourier Transform from 12-2400samples[6].In the forthcoming 5G,FFT remains a really necessary algorithm for all of the waveform candidates. Thereforethe FFT consumption speed ought be high enough to support the high FPGA implementations to form utilize of those present technologies of information transmission and it's essential to build up the proficient technique of digital modulation.

II. LITERATURE SURVEY

In this survey, it is provided that the maximum throughput is calculated by the utmost bandwidth by multiply the no. of streams that one FFT processor handles. In the earlier designs, they presuppose that one FFT processor which supports at most 8-stream 2048-point FFT consumptions. The processor supports a throughput of 983.04MS/s, where the cyclic prefix samples don't seem to be detached. Therefore RqOnThrpt is overestimated. The hardware intend supported the constraint which can provide sufficient performance for 5G. Fast Fourier Transform is an algorithm which has been projected by Cooley and Tukey[1] to compute Discrete Fourier Transform that converts the time domain to the frequency domain and reduce the complexity of time also to O(Nlog 2N).In real-time systems, the foremost thing is speed of the processor which is being executed. Based on this, several architectures are taken place like architecture having single memory and as well as double memory architectures.

Generally, the architecture of pipeline FFT processor are classified into twono.of categories.

1.Single-path delay feedback pipeline architecture.

2.Muliple-path delay commutator pipeline architecture.

In this paper, Multipath Delay Commutatorvarieties the opinion path into feed-forward streams expending switches boxes together with the memory scheduling which are being used to implement a Fast Fourier Transform in the OFDM.

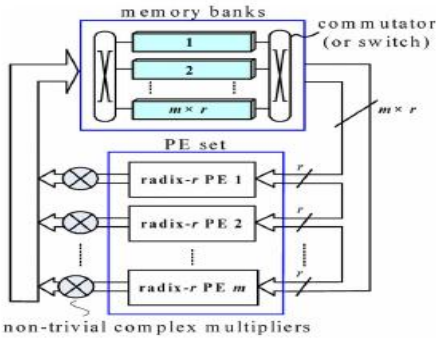


Fig.1. Architecture of General Memory-Based Architecture.

Fig.1. Shows the Memory Based Architecturewhich can't be parallelized where the pipeline design architecture can be overwhelmed the disadvantage of the previous one comparing to previous designs.[13].pipeline based architectures works in real-time processing , continuous processing and consuming smaller latency with less delay which are required for furthermost of the applications. The architecture which is compared with pipelined butterfly architecture is set in place of memory based architecture with general memory based architecture contains radix-r butterfly units.

III. DESIGN CONSIDERATIONS

REQUIREMENTS OF 5G:

TABLE-1
SCALABLE OFDMNUMEROLOGY FOR 5G NR (3GPP RELEASE 15)[14],[2].

Subcarrier Spacing	15 kHz	30 kHz	60 kHz	120 kHz
Frequency Band	0.45-6GHz	0.45-6GHz	0.45-6GHz, 24-52.6GHz	24-52.6GHz
OFDM symbol duration	66.67us	33.33us	16.67us	8.33us
Cyclic prefix duration	4.69us	2.34us	1.17us	0.59us
OFDM symbol with CP	71.35us	35.68us	17.84us	8.91us
Maximum bandwidth	50 MHz	100 MHz	200 MHz	400 MHz

Table-1enumerates the relation between subcarrier spacing and the OFDM characteristics which describe the implementation ofthe system. It should be taken into account that the subcarrier spacing of 60 kHz is the only one that can describe both 0.45-6 GHz and 24-52.6 GHz intervals.

The requirements of 5G are given in Table-1 above.Besides the above-presented parameters, another important value is the maximum number of active subcarriers. The maximum number of subcarriers are being achieved at the maximum bandwidth of 450 MHz for an FFT value of 4096, where the number of users active subcarriers is 3276. Although 3276 is the maximum currently achieved number, the largest possible value is 3300 subcarriers. The used waveform type for 5G NR is CP-OFDM on both downlink and uplink. This choice creates a reduced complexity model for the communication system between the central system and the local networks. The total no.of active subcarriers are 3276 for all numerologies, which leads to the maximum bandwidth enabled by the parameters described in Table 1.

A. Design Space Exploration:

In this design, the previous reference architecture is about memory based architecture with the help of a radix-r butterfly units. The proposed architecture is enhanced and designed a RAM and ROM based technologies and supported the previous architecture which is considered as a reference. Here we assume 16-stream 4096-point FFT processor computation stages. The necessity for throughput is to be calculated based on the reference architecture and obtain a value of 1966MS/s. comparing with the reference architecture the Requirement on latency for 16-stream 4096-point FFT computations is very much lesser than 4ms and which are more adequate for 5G.

IV.PROPOSED ARCHITECTURE

The proposed architecture is designed by using Radix2^2 algorithm consists of RAM units, Butterfly units and this architecture acts as a distributer and distributes the allocated resources to the user. In reference with the base paper we designed this RAM and ROM based FFT processor. Previously only transmitter is designed and by considering the base paper we designed a receiver and this architecture will be kept on the receiver side of the OFDMA communication system. To achieve the speed and the throughput of the processor the inputs of the architecture are given the multiple choices for the proposed architecture. The proposed architecture consumes almost 53% lesser power in comparing with the previous deigns.

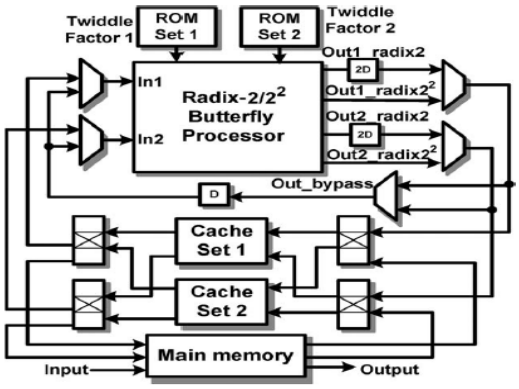


Fig.2. Architecture of proposed Programmable FFT processor.

Fig.2. shows the designed architecture RAM and ROM based architecture with dual port memories and radix butterfly processor. This design exploits dual SRAM in familiar with the FFT kernel. Moreover the FFT kernel which has been inside executes four-path data operations .While the communications stuck between the fft kernel and the memory involves the eight-data path admittance and single port SRAM which can be useful through discrete "read and write" operations. Thus here the memory area can be efficiently reduced using this proposed architecture.

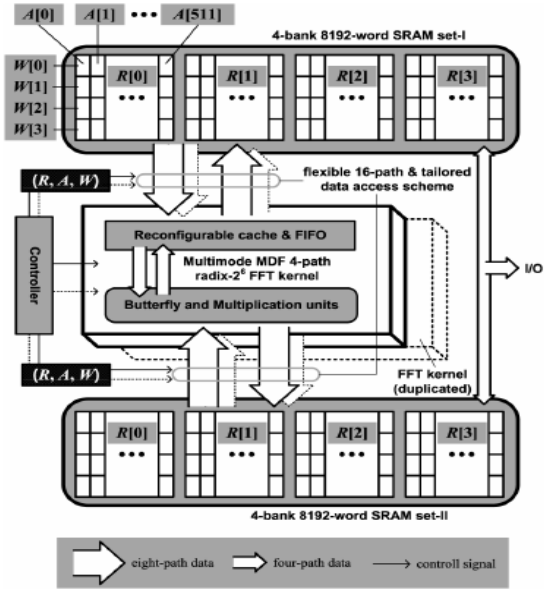


Fig.3. FFT Hardware Architecture using Dual port SRAM.

Fig.3.shos the four word data width in the SRAM, one or two groups of eight paths associated with one or two FFT kernel can be accessed.

A. The Overall Design Of The FFT Processor Architecture:

The FFT module is one of the major important block in the OFDMA system method. In this system the fundamental module of the OFDMA substantial layer be the FFT module, which are able to be used in the FFT points 4096 points,2048 Points, 1024 points,512 points, 128 points and 64 points. The overall intend of the variable point FFT processor has simply supported the FFT component presented inside the OFDMA system application. Agreeing to the knowledge of Fourier algorithm which is 2-dimensional, i.e. N1=2, N=128, N2=64. We determine when we achieve 128-point FFT by multiplying the above calculations. Initially the data is structured in a 64 lines and a couple of rows, Next, the input file will transform the 64-points FFT, then the obtained result will perform 2 points FFT. Similarly to calculate the 512-point FFT. Primarilywe perform the 64-points FFT then transfer to 8 points FFT. The same method can be used to calculate the 2048 and 4096 points FFT.A building block diagram of the on the whole design of the FFT processor is shown in Fig.3 .In this the simulation is done with the help of Verilog language.

B.64-Point FFT Component

This module is theutmost often use in this design. There are four kinds of input data length. These input data must firstly passes by the 64-points FFT module. The equivalent thought within the module supported 2D Fourier transform algorithm be made of two 8-point FFT modules. As a result the 16-point FFT module is taken into account which is kernel in this part, here its recital which disturbs the entire design .The 16-point FFT processor structural design consists of one 2^2 butterfly ,a dual port FIFO RAM, a coefficient ROM, and a controller and an address generation unit.

C. Select And Power Module

This portion belongs kernel to inclusive the data measurement lengthwise in this particular design.It is maintained the input file point is to pick the results and stored within the middle data memory, then decide the way to the next flow. A signal two bits 'mode' is always selected here because the manner signal which is chosen can be denoted with the given values like when mode=00, means to settle on a 2 points FFT component, to finish the 128-point FFT, while the mode=01 means to finish the 2048-point FFT, when mode=11 way to finish the 4096 points FFT.

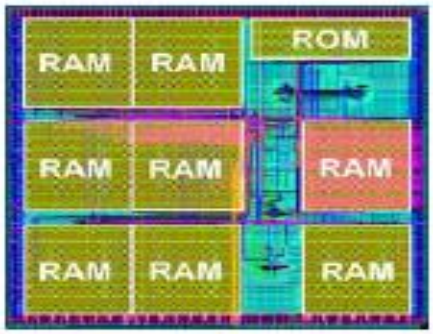


Fig.4. Physical layout of the FFT processor

Fig.4. shows a physical layout of the FFT processor where it consists of dual-port RAM and ROM.

TABLE-II

FFT Processor Comparison With Register And Memory

Stage:	register-based (mW)	RAM-based (mW)
1	5.39	4.59
2	9.84	8.79
3	5.13	4.64
4	2.75	2.55
5	1.57	1.52
6	0.96	1.01
7	0.69	0.73
8	0.47	0.51
9	0.32	0.36

V.LOW POWER CONSUMPTION CALCULATIONS

An FFT Processor Architecture is synthesized in smaller technology then the result is also reduced. To compensate the difference in this technology, the Normalized area is considered and calculated below by using 130nm technology. Normalized Area= Area/(Technology/130nm)^2

- (1)

TABLE-III Comparison Table Of Normal Memory Based Architecture With Proposed Memory Based Architecture

ITEMS	NORMAL ARCHITECTURE	PROPOSED ARCHITECTURE
FFT SIZE	12-2400 POINT	16-4096 POINT
PROCESSOR TECHNOLOGY	65nm	130nm
FREQUENCY	250MHz,250MHz	450MHz,1GHz
AREA	1.46mm^2	1.21mm^2
DELAY	4.69ns	5.962ns
POWER	68.64mW	32.16mW

TABLE-IV

System Implementation Values Using Xilinx

Parameter	Value
FFT Points	4096
Modulation	64-QAM|256-QAM
NPayloads	1
Fc	0.45-6 GHz and 24-52.6 GHz
Bandwidth	450MHz

VI. LOW POWERIMPLEMENTATION METHODS

During power dissipation the CMOS transistor will depends on the capacitance, supply voltage and therefore the speed at where the information toggles.

$$P=f*C_{load}\,VDD^2 \qquad -(2)$$

Here,

C_{load} is the capacitance of the load of a CMOS transistor.

VDD is the supply voltage

F is the frequency

Ex: 1 Sqnr Calculations as per data sheet rule of thumb, that each bit more gives you about 6 dB more SNR.

Apply A/2 rules

$$SQNR_{dB}=10*10\log_{10}(2^{2N}/C^2) \qquad -(3)$$

$$SQNR_{db}=3.01*14=42.14\ dB \qquad -(4)$$

TABLE-V

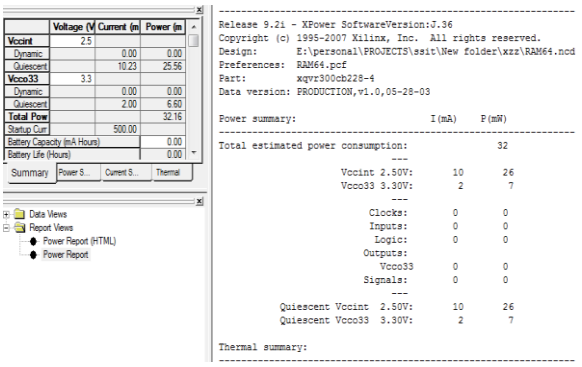
SYSTEM PARAMETERS FOR WLAN, 4G, AND 5G[15]

Standard	Waveform	FFT Sizes	Modulation	Maximum Bandwidth
802.11n/ac	OFDM	64-512	up to 256 QAM	160 MHz(512 point)
4G LTE/LTE-A	OFDM	128-2048/1536 12-2400	up to 256 QAM	30.72 MHz (2048 Point)
5G	OFDM	up to 4096	up to 256 QAM	400 MHz (4096 Point)

TABLE-VI

FFT PROCESSOR POWER CONSUMPTION (a)

	Voltage (V	Current (m	Power (m
Dynamic		0.00	0.00
Quiescent		10.23	25.56
Vcco33	3.3		
Dynamic		0.00	0.00
Quiescent		2.00	6.60
Total Pow			32.16
Startup Curr		500.00	
Battery Capacity (mA Hours)			0.00
Battery Life (Hours)			0.00



(b)

VII. SYNTHESIS RESULTS

In synthesis results of this processor is illuminated in detail. Ahead of the time, the quality of hardware synthesis flow which has been adopt in generate a net list and estimate the parameter like gate count, delay, area and power. Synthesis results are generate by by means of Xilinx. The technology which was used is 130nm COMS technology and the bandwidth applied is 450MHz, and the area occupies is 1.21 mm^2 and the power consumption is 32.1mW, at this point we had chosen the processor capability which is proportional an arrange of a 4096-point FFT. The twiddle factor is one of the driven approaches, and is one of the advantages. Whenever it is not required it can be turn off.

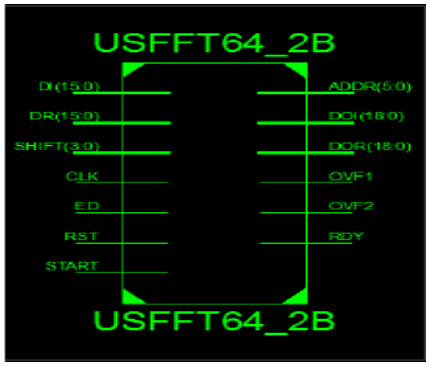


Fig.5. Programmable FFT processor synthesized RTL schematic.

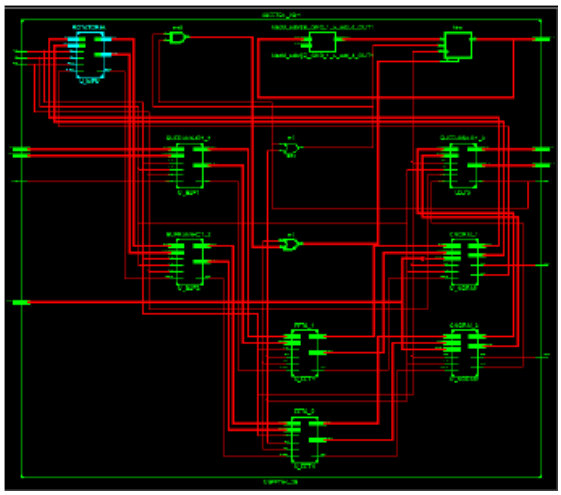


Fig.6. shows the internal structure of the synthesized PFFT processor whittle which is to be obtain after simulation and synthesizing the High speed FFT processor for OFDMA system using FPGA.

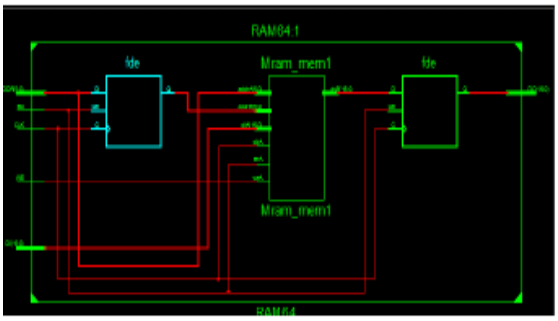


Fig.7.Internal Unit Design (memory)

Fig.7. shows the Memory internal unit design of 64-bit RAM.

VIII. SIMULATION RESULTS

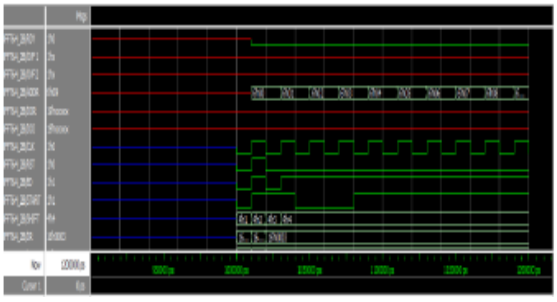


Fig.8. FFT Processor simulation output

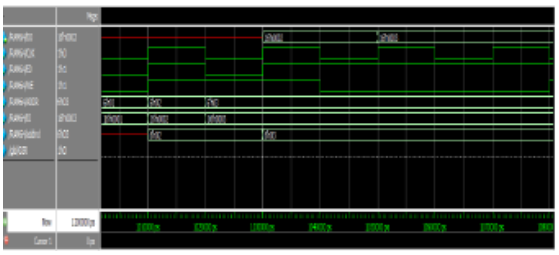


Fig.9. FFT Processor Memory unit simulation output

Fig.9.shows the memory unit simulation of 64-bit RAM,where dual-port RAM is taken into consideration for output.

Data flow structures _1

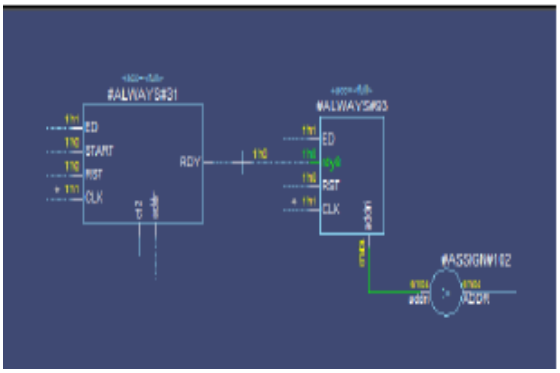


Fig.10. FFT Processor Memory unit Dataflow output.

Fig.10. shows the FFT processor Memory unit design dataflow output by using RAM and ROM memory.

Data flow structure_2

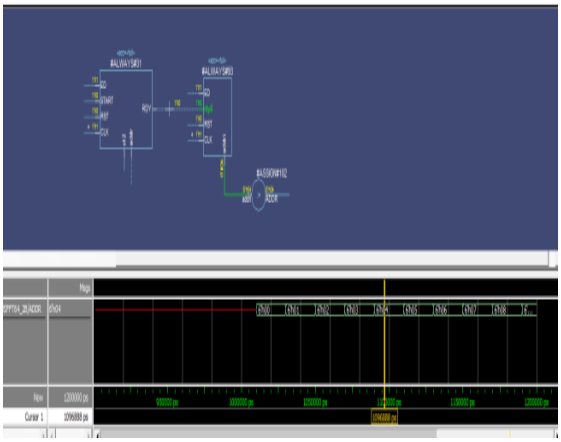


Fig.11. FFT Processor Dataflow output

Fig.11. shows the Final Dataflow output where we can calculate 16-4096 point FFT computations.

USFFT64_2B Project Status (11/14/2019 - 17:01:28)			
Project File:	hema.xise	Parser Errors:	No Errors
Module Name:	USFFT64_2B	Implementation State:	Programming File Generated
Target Device:	xc3s100e-5vq100	• Errors:	
Product Version:	ISE 13.2	• Warnings:	
Design Goal:	Balanced	• Routing Results:	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• Timing Constraints:	All Constraints Met
Environment:	System Settings	• Final Timing Score:	0 (Timing Report)

Device Utilization Summary				[-]
Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Flip Flops	6	1,920	1%	
Number of occupied Slices	3	960	1%	
Number of Slices containing only related logic	3	3	100%	
Number of Slices containing unrelated logic	0	3	0%	
Number of bonded IOBs	41	66	62%	
Number of RAMB16s	1	4	25%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	1.28			

Fig.12. Device Utilization Summary Report(Area report)

Fig.12. shows that the device utilization area summary report. In the previous design, the area occupied is 1.46mm^2 and in this design, we show that the area is reduced to 1.21mm^2.

```
================================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'CLK'
  Total number of paths / destination ports: 16 / 16
--------------------------------------------------------------------------------
Offset:              5.962ns (Levels of Logic = 1)
  Source:            Mram_mem (RAM)
  Destination:       DO<15> (PAD)
  Source Clock:      CLK rising

  Data Path: Mram_mem to DO<15>
                               Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     RAMB16_S18_S18:CLKB->DOB15    1   2.436   0.357  Mram_mem (DO_15_OBUF)
     OBUF:I->O                 3.169          DO_15_OBUF (DO<15>)
    ----------------------------------------
    Total                      5.962ns (5.605ns logic, 0.357ns route)
                                       (94.0% logic, 6.0% route)

================================================================================


Total REAL time to Xst completion: 3.00 secs
Total CPU time to Xst completion: 3.17 secs

-->
```

Fig.13. Device Utilization Summary Report(Delay Report)

Fig.13. shows the delay report which is 5.96ns when compared to previous designs it is a bit higher.

```
--------------------------------------------------------------------
Release 9.2i - XPower SoftwareVersion:J.36
Copyright (c) 1995-2007 Xilinx, Inc.  All rights reserved.
Design:       E:\personal\PROJECTS\ssit\New folder\xzz\RAM64.ncd
Preferences:  RAM64.pcf
Part:         xqvr300cb228-4
Data version: PRODUCTION,v1.0,05-28-03

Power summary:                          I(mA)     P(mW)
--------------------------------------------------------------------
Total estimated power consumption:                  32
                                         ---
                        Vccint 2.50V:       10       26
                        Vcco33 3.30V:        2        7
                                           ---
                             Clocks:        0        0
                             Inputs:        0        0
                              Logic:        0        0
                            Outputs:
                               Vcco33       0        0
                            Signals:        0        0
                                           ---
              Quiescent Vccint  2.50V:       10       26
              Quiescent Vcco33  3.30V:        2        7

Thermal summary:
--------------------------------------------------------------------
```

Fig.14. Power consumption reduced more than 53%

Fig.14. shows the power consumption which is reduced by more than 53%(32mW) comparing with previous designs (68.64mW). This is the main advantage of this design.

IX. HARDWARE IMPLEMENTATION

Synthesis process would also produce a bit stream file that can be downloaded in the ZynqUltraScale +MPSoC board. The bit stream file of the Programmable Fast Fourier Transform has been successfully downloaded to the diligent Xilinxfamily of the board after installing necessary drivers on PC. The test operation of the physical functionality of the Programmable FFT has been done by simply interfacing a function generator to apply input data and oscilloscope to monitor the recovered data.

X. IMPLEMENTATION RESULTS

After compiling the VERILOG code by using Xilinx14.3 and downloading the bit-streams successfully to the ZynqUltraScale+MPSoC board, TTL data from function generator of rate 1 GHz frequency has been applied to the board and 450MHz frequency is applied on FPGA and 650MHz is applied on the Zynq board.while the output has been measured by an oscilloscope. Output data will be obtained when the input to the control circuit is given as logic 1. The power consumption is condensed more than 53% (32.16mW) compared to the existing system and SQNR is obtained as 42.14dB.

XI. CONCLUSION

Programmable FFT processor using Dual RAM and ROM technology is proposed for 5G communications. This architecture uses a memory-based FFT processor which supports 12-2400 points and 16-4096 point Computations for 4G and 5G communications. In the upcoming 5G we require less area and as well less power consumption so we have an advantage by using this dual Ram and Rom technology which can reduce area and power by applying 1Gz Frequency to 3.5GHz frequency where the 5G band starts from MHz to GHz FFT processor with dual Ram and Rom technology is the suitable way. The processor is designed uses Verilog *language* to simulate the path using Xilinx software to put together this model and to authenticate Timing analysis diagram on Mentor Graphics(Model Sim).The results show the power and are reduced comparing to previous architectures.

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