



The Effect of Doping on Different FET Structures: MOSFET, TFET and FinFET

Anjali Goel, Neelam Rup Prakash

Abstract: MOSFET have been scaled down over the past few years in order to give rise to high circuit density and increase the speed of circuit. But scaling of MOSFET leads to issues such as poor control gate over the current which depends on gate voltage. Many short channel effects (SCE) influence the circuit performance and leads to the indeterminist response of drain current. These effects can be decreased by gate excitation or by using multiple gates and by offering better control gate the device parameters. In Single gate MOSFET, gate electric field decreases but multigate MOSFET or FinFET provides better control over drain current. In this paper, different FET structures such as MOSFET, TFET and FINFET are designed at 22nm channel length and effect of doping had been evaluated and studied. To evaluate the performance donor concentration is kept constant and acceptor concentration is varied.

Keywords: Doping, FinFET, gate voltage, MOSFET, TFET and threshold voltage.

I. INTRODUCTION:

In modern day integrated circuits, MOS transistors have gained popularity over conventional transistors because of its properties like low power consumption, high speed and high input impedance. Moore's Law led to extensive research in downscaling of transistor parameters. Downscaling of transistors parameters had led to increase in operating speed, low power consumption and reduction in die area of prevailing integrated circuits. To cope up with this law, the channel length of MOSFETs has been lowered gradually in past few decades [1]. However, lowering of channel length beyond a certain level leads to degraded performance of MOS transistors. Performance degradation occurs due to effects like Drain Induced Barrier Lowering (DIBL), Gate Induced Drain Lowering (GIDL), subthreshold leakage and enormous parameter variations. These effects are known as short channel effects (SCE) [2, 3]. Scaling of MOSFET leads to decrease in threshold voltage (V_{th}) thereby causing escalation of leakage current. These SCEs restrict the downscaling of MOS device beyond a certain level without tolerable degradation in its performance [4]. To elucidate these problems, various device structures and working mechanisms had been proposed, one of which, that gained much attention is TFET (Tunnel Field Effect Transistor).

In TFET the carriers tunnel from source to channel via quantum mechanical tunneling whereas in MOSFET charge injection takes place through thermionic emission [5-6]. The conventional TFET concentrates only on dc transfer characteristics at device level particularly during the increase in the number of interconnect parasitics in the device as equated to gate parasitics.

The VTFET are alike to conventional TFET in respect of flow of carriers but VTFET overcomes the shortcomings of conventional TFET.

The VTFET has sharper subthreshold slope (SS) which is disadvantageous in conventional TFET. The sharper SS leads to decrease in OFF current and also enhances performance of low power electronic devices [7-8]. FinFET overcomes the drawback of SCEs by having higher dominance of gate over channel.

Along with that when compared to TFET, it has improved ON/OFF property. FinFET also has reduced leakage, minor erraticism, and exceptional electrostatic command over channel and decreased power consumption. For high-performance application, FinFET is preferred over TFETs [9]. The rest of paper is organized as follows: Section II summarizes the previously reported FET structure and their shortcomings.

Section III explains the FinFET and TFET devices structures and Section IV explains the Design Considerations of TFET and FinFET fabrications. Section V explains the device structure and simulation. Finally section VI highlights the summary of the paper.

II. II PREVIOUSLY REPORTED FET STRUCTURES

The International Technology Roadmap for Semiconductors (ITRS) is a manuscript that described the inventions in the field of IC technology over the past 20 years. The main objective was to assist the industry to endure productivity and evolution of Moore's Law.

ITRS reflects the headway generation of IC technology, offers the communal reference for the semiconductor industry.

The objectives achieved in the Roadmap were required to be authenticated but bellicose at same time [10].

Figure 1 illustrates the downscaling of feature size of transistors with time. It can be seen that reduction is exponential with time.

Although, the present-day technology permits solid matter to be fashioned at various levels like molecular and atomic. Thereby, the manufacturing and usage of Nano-Scale devices had become realistic [11].

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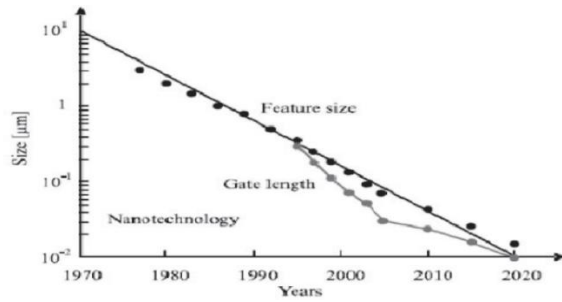


Figure 1: Feature Size of Transistor as a function of time [11]

These roadmaps were anticipated to increase innovations within the industries. The reduction in the size of MOSFET led to intensification of the operating speed, packaging density and functionality of IC's. The gradual reduction of device size results in SCE's, enlarged subthreshold leakage current and threshold voltage reduction as an outcome of adjacent immediacy between source and drain. Along with this, the performance of device also lessens due to rise in power consumption. Static power and dynamic power are two modes of power consumption appears in IC's [12]. As the size of the device further reduces, the temperature independent current mechanism is required which lacks in MOSFET. In MOS transistors, when there is change in gate voltage to change drain current while operating in subthreshold region, it is depicted by the following expression:

$$\frac{KT}{q} \ln(10) = 60 \text{ mV/decade at } T=300\text{K} \dots \dots (1)$$

To keep the overdrive voltage high at reduced channel length, it was essential to lower the value of V_{dd} and V_t . Therefore, to overcome the drawbacks of MOSFET, the TFET was exploited. TFETs can achieve the lower value of subthreshold swing than MOSFET [13]. The prime difference between them was their working mechanism. In MOSFET, charge carriers move from source to drain via thermionic emission whereas, in TFET, movement of carriers is based on the band to band tunneling (BTBT) phenomena. Figure 2 shows the divergence in the transfer characteristics of MOSFET and TFET. It has been witnessed that, TFET's were not limited by thermal Boltzmann extremity of carriers because of its BTBT phenomena and possess the capability of delivering subthreshold-swing below 60mV/decade at room temperature. It was also inferred that in TFET the OFF current and operating voltage decreases because of drop in SS in the subthreshold region.

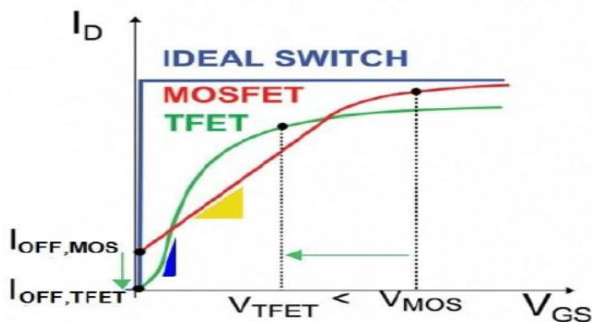


Figure 2: Divergence of Characteristics of MOSFET and TFET[14]

In 2013, ITRS had envisaged that TFET would remain a research issue till beginning of 2020s before they would be manufactured and utilized for low power applications [14]. TFET's proven to be useful in the field of low power applications but it has certain disadvantages as well. It experiences struggle in retaining sudden tunneling junctions because of diffusion of dopants [7]. It also has high ON/OFF property. The drawbacks of TFET were overpowered by FinFETs because they possess lower ON/OFF property. FinFET is a tri-gate device whose conducting channel is enfolded by a thin silicon film from which it has received its appellation. The width of the fin outlines the effective channel of the device. It can regulate the channel from all the sides of the gate. Due to the ability to regulate the channel from all the side of the gate it overcomes all the minuses of SCE's. It has reduced leakage, exceptional subthreshold ascent, rapid speed of exchange and lesser power consumption [15]. Figure 3 demonstrates the improvement in SCE's accomplishment of FinFET in contrast to planar MOS structure.

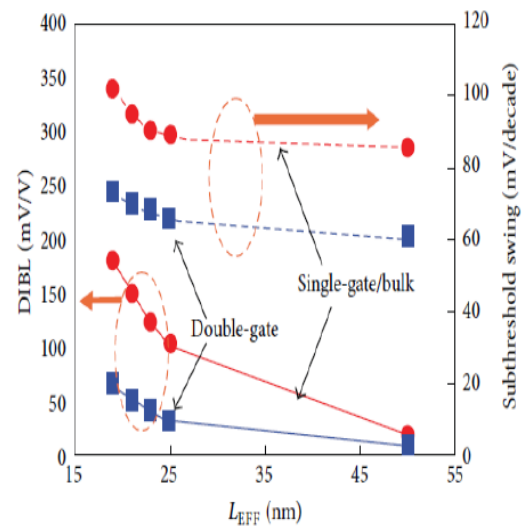


Figure 3: Variations of SCE's w.r.t channel length [16]

The conventional MOSFETs when operating at reduced channel has various drawbacks in terms of its performance in low power applications, leakage currents, SCE such as DIBL, GIDL and speed issues that had led to degradation of MOSFET. In order to maintain the constant electric fields while reducing the MOSFET dimensions channel length and oxide thickness had been scaled by $1/K$ and doping was increased by factor K . This scaling of dimensions result in scaling of applied voltage by $1/K$ factor. This type of scaling was termed as R. Dennard Scaling [17]. But R.Dennard scaling was not applicable for non-planar devices because gate overdrive changes due to variations in supply voltage and threshold voltage. Since threshold voltage is proportional to channel length. The shortcomings of conventional MOSFETs led to the development of TFETs. TFETs were proven to be useful for low power applications. Ion/Ioff current ratio is high for TFET and they possess low subthreshold leakage current which led to less leakage per device. For scaled TFET device, gate overdrive increases leads to increase ON current.

Prior experiments on TFET, demonstrates that for 50 nm node, on current was of the order of 0.5-0.7 mA and off current of the order of 10 pA [18,19]. Additional improvement was required to optimize the ON state current and prevent ambipolarity as transistor size was decreased. To overcome this FinFET structure was proposed by Hisomato et. al. in 1989[20]. FinFETs has vertical channel known as FIN. The channel length in FinFET is related to Fin height characterised as width optimization. Therefore, on state current could be increased by varying Fin height and number of fins [21]. For channel length below 10 nm, FinFET power is 50% lower than TFETs. FinFETs were proven better for high performance and low power applications [9].

III. III TFET AND FINFET DEVICE STRUCTURE

3.1 TFET Device Structure

The basic layout of TFET is analogous to the MOSFET excluding that source and drain terminal are incapacitated with reverse type and the most extricate characteristics of TFET is nobbling used for drain and source. A communal TFET device structure comprises of a p-type, intrinsic, n-type junction led to formation of p-i-n diode, inside which the electrostatic potential of the inherent region is regulated by a gate terminal and it operates in the reverse bias condition. Thermal injection is a process for the source of carrier inoculation used in MOSFET whereas TFET operates the BTBT process of charge carrier. TFET basic structure comprises of three portions (source, drain and gate). Source terminal is utilized as a cause of majority carrier. Drain terminal is utilized to transmit the majority carrier and Gate terminal is utilized to regulate the majority carrier flowing from source to drain ramblingly regulating the drain current. Channel is molded in-between the p-type and n-type region. Gate oxide is utilized to cloister gate and to allow gate to regulate the electrostatic in the channel and oxide is cloister; gate oxide averts the current leakage from channel to gate. Figure 4 displays the representation of p-i-n TFET [22].

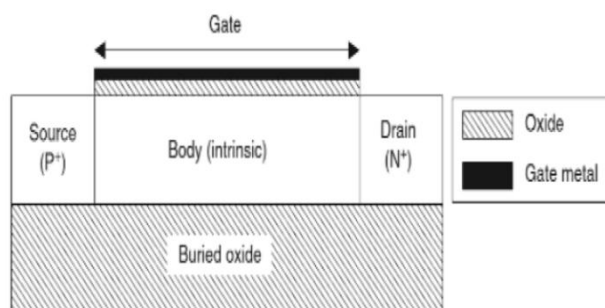


Figure 4: Representation of p-i-n TFET [22]

These are also known as gated p-i-n diodes. To enable the device, the diode is reverse biased and a voltage is supplied to the gate. Reverse bias is essential for tunneling effect and along with that it had been observed that N-MOS functions when positive voltage are given to gate and drain. Thus, n-region of TFET is denoted as its drain and p+ region as its source for n-type device. The TFET's metal gate operates on work function of 4.5eV. Figure 5 illustrates the structure of p-i-n TFET.

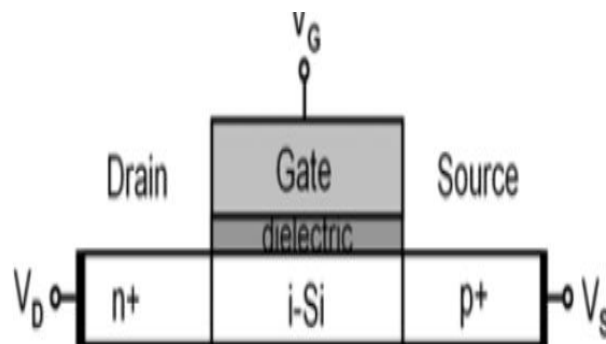


Figure 5: Structure of p-i-n TFET[23]

It has sharper switching nature, works on BTBT mechanism [23]. It has capability of having subthreshold swing lower than the 60mV/decades, overcomes the problems of SCE's, minimizes the leakage currents, crosses the speed necessities because of tunneling effects and also has higher ON/OFF current ratio [24].

3.2 FinFET Device Structure:

FinFETs are evolving technology in the present scenario. They has assorted design choices and improved regulation over the channel leading to reduced power structures and advanced noise lenience. The FinFET device design includes of a silicon fin enclosed by shorted or independent gate on any side of the fin usually on silicon insulated substrate. It has two gates which can operate either self-sufficiently or when coupled together. The voltage at one gate can be regulated by the voltage at another gate. Figure 6 illustrates the FinFET in various schemes.

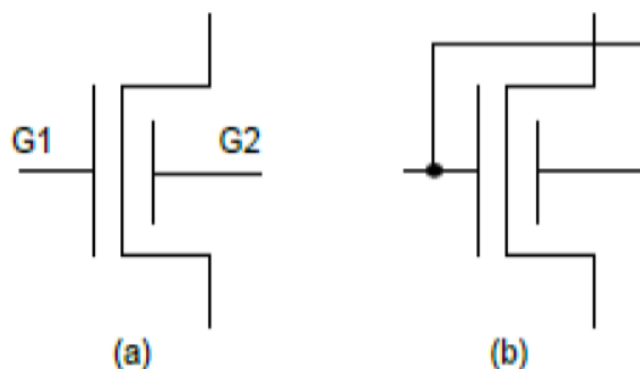


Figure 6: FinFET schemes (a) self-sufficient (independent) gates (b) united (shorted) gate [25]

These devices can be utilized to rise the performance by decreasing the leakage current and power dissipation as front and back gates both can be regulated self-sufficiently or when coupled together [25]. The movement of charge can be enhanced by aggregating the amount of fins on the device which provides improved gate regulation on the channel charge. The fin height is quantifiable factor to describe the stability of the device [20]. The profits of FinFET are that they have less cost, reduced SCE, increased technological adulthood and have abilities of matching [26]

IV. DESIGN CONSIDERATIONS OF TFET AND FINFET

4.1 Design Consideration and Optimization of TFETs

Although, TFETs possess high ON/OFF current ratio but various key issues needs to be considered while designing the TFET.

4.1.1 Single and Double gate TFET's

Conventional TFETs possess low ON/OFF current ratio. In order to offer enhanced electrostatic control over the channel, number of gates in devices had been increased. TFET with double gate or multigate deliver high I_{on} . Second gate in TFET is created at the bottom of single gate TFETs [27]. Single gate and double gate TFETs are illustrated in figure 7:

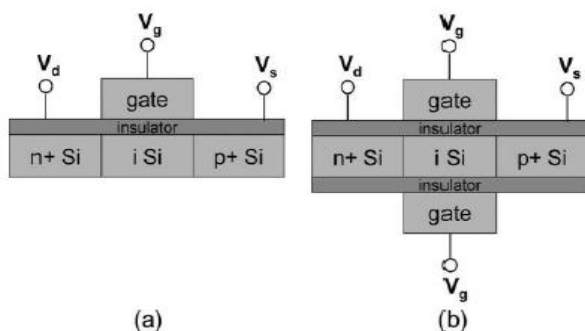


Figure 7 (a) Single TFETs (b) Double gate TFETs

Double gate(DG) TFETs offers improved transconductance and lessened threshold voltage. By selecting appropriate gate dielectric, DG TFET's can poses low threshold voltage roll-off, high I_{on} and reduced I_{off} as compared to conventional TFETs. The supply voltage of Ge based TFET was limited to 0.5 V for circuit level designs [28].

4.1.2 Asymmetric Gate Oxide

Nagpal et al in 2012, observed the performance of asymmetric gate oxide DG TFET with a high-k dielectric at source region and low-k dielectric at drain of TFET. The high gate grain capacitance of DG TFET is controlled by replacing SiO₂ with air (k=1) at the drain side resulting in higher cut off frequency. DG-TFET with asymmetric gate oxide had been reported best for low power applications at circuit level [29]. Figure 8 shows the DG TFET with asymmetric gate oxide

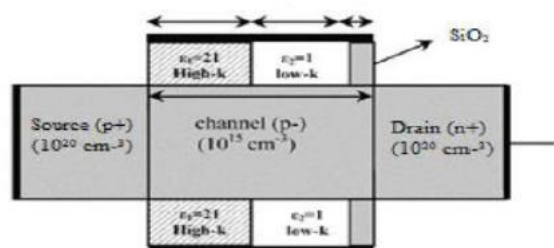


Figure 8: DG TFET with asymmetric gate oxide [29]

4.1.3 Gate on Drain Overlap

The movement of electrons and hole in opposite direction can be suppressed with gate-drain overlap in TFET. In TFET, even at higher drain doping level ($1 \times 10^{19} \text{ cm}^{-3}$) ambipolar conduction can be suppressed. Band bending of device doesn't get altered at higher drain doping levels because of gate potential in overlapping regions [30]. Figure 9 depicts the gate on drain overlap structure of DG TFET.

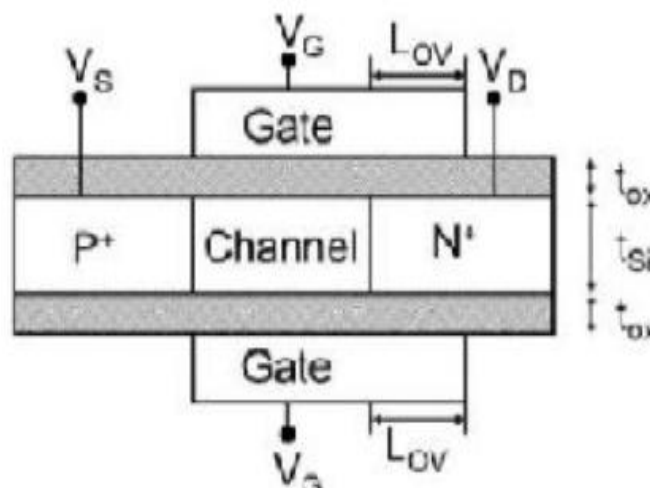


Figure 9: Gate on Drain overlap structure [30].

4.2 FinFET Design Challenges

Various parameters of device technology is influenced by downscaling of device and modification in device architecture. Below are some of the key issues.

4.2.1 Fin Patterning

In order to achieve the matched or exceeded width of FinFET device either their fins needs to be extremely tall or huge number of fins should be gathered per pitch. Normally, two fins per each base pitch provides a tolerable fin aspect ratio that helps to achieve either matched or exceeded width as compared to planar device. Lithographic designing of such fins has few drawbacks associated with it:

Overlay error may appear between two fins pattern because of double patterning required for splitting the base pitch. This error could lead to undesired fin pitch variations that influences down-stream handling.

If selected fin width is smaller than twice the gate length, it may result in intolerable capabilities of optical lithography leading to poor fin width control [31].

4.2.2 Orientation of Fin

Current in FinFET drifting along $\langle 110 \rangle$ sidewalls is because of alignment of fins in direction $\langle 110 \rangle$ on wafers $\langle 100 \rangle$. Along $\langle 110 \rangle$ direction, hole mobility is usually higher on $\langle 100 \rangle$ wafers but as stress is employed difference between electron current and hole current decreases. In non-planar device such as FinFET electron mobility is higher along $\langle 110 \rangle$ surface than along $\langle 100 \rangle$ sidewalls. For uniform thickness if Fin either epitaxial layer can be used or diamond shape structures could be extended on $\langle 110 \rangle$ sidewalls [32].

4.2.3 Fin measurement variability

Effective width of FinFET device is directly proportional to fin height. Out of the two parameters, fin height is more crucial. Any modification in fin height and shape is transferred to device width difference. FinFET devices suffer from device width variations whereas in MOS devices, design variations only affect the narrowest of transistors [33].

4.2.4 FinFET parasitic capacitance

Parasitic capacitance of FinFET device is usually higher than planar devices such as MOSFETs. Gate to fin capacitance includes capacitance of gate above the fin and the top of fin. This capacitance reduces with increase in fin height and decrease in fin pitch per effective width of device. Junction capacitance of Bulk FinFET between source/drain area and well/substrate was reported several times lesser than MOS devices [34].

V. V Device Structure and Simulation

5.1 MOSFET Structure

For a given MOSFET structure the V_{th} can be related to SCE and DIBL by the following equation:

$$V_{th} = V_{th0} - \text{SCE} - \text{DIBL}$$

where V_{th0} is the threshold voltage of a long channel device, SCE is short channel effect and DIBL is drain induced barrier limiting. The reduction in threshold voltage along with decrease in gate length is a popular SCE called “threshold voltage roll-off”. The MOSFET realized has gate length equals to 22nm which is formed by diffusing the drain and source. Thickness of gate oxide layer, acts as insulator is 2 nm and is made up of SiO_2 . Figure 10 illustrates the MOSFET structure realized at 22nm gate length and table 1 dictates the different regions of MOSFET with their meshing size.

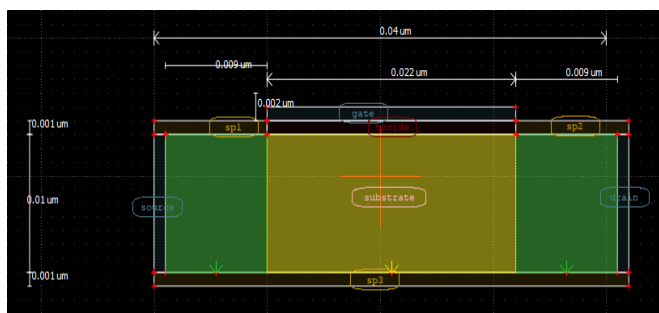


Figure10: Structure of MOSFET having channel length 22 nm

Table 1 Different regions of MOSFET

Region	Material	Mesh Size
Substrate	Silicon	0.005
Soucre/Drain	Al	0.001
Oxide	SiO_2	0.0005
Spacers	Nitride	0.001
Gate	Al	0.002

5.2 TFET Structure

The TFET uses the MOS gate to achieve BTBT. The device is off when zero gate volatge is applied and BTBT is suppressed during that time. The gate length is 22nm and it is made using NPolySi and gate oxide thickness is 4nm. Gate material has significant effect over drain current where as source and drain material doesn't affect the properties of TFET. The TFET structure under study is demonstrated in Figure 11 and table 2 dictates the various regions of TFET with their meshing size.

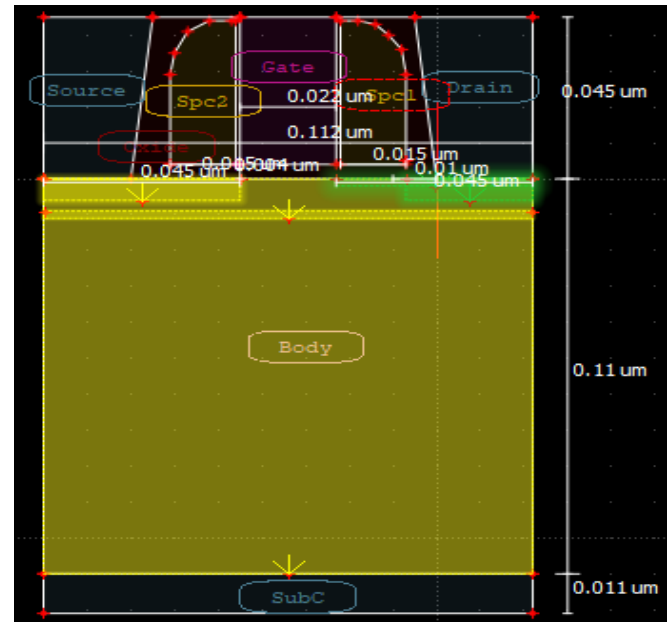


Figure 11: TFET structure under study

Table 2 Different regions of TFET

Region	Material	Mesh Size
Source/Drain	Al	0.005
Gate	NpolySi	0.003
Oxide	SiO_2	0.004
Substrate Contact	Al	0.004
Substrate	Silicon	0.005
Spacers	Nitride	0.004

5.3 FINFET Structure

For two-gate FinFET, effective channel length (ECL) is given by

$$\text{ECL} = 2H_{fin} + T_{fin}$$

Where H_{fin} is height of FinFET and T_{fin} is thickness of FinFET. Two-gate FinFET has both the gates aligned on both faces of the fin fixed by H_{fin} and a gate increased above which is equal to T_{fin} . So, the gate length is 22nm and H_{fin} is 2nm, so according to calculations T_{fin} i.e. width of gate is 18nm.

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The gate insulators are made up of high-k dielectric spacers (sp1,sp2,sp3,sp4). Both the gate oxides (toxide/boxide) are made up of SiO₂ and thickness of gate oxide is 2nm. The structure of FinFET is shown in Figure 12

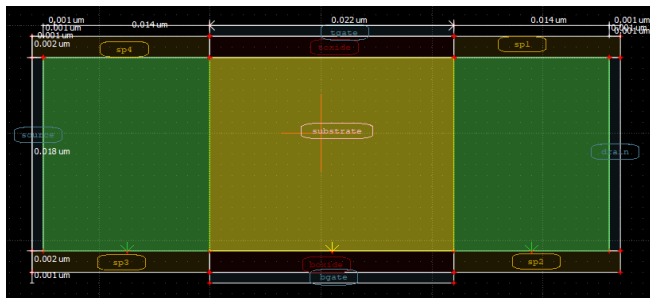


Figure 12: FinFET device structure

Table 3 Different regions of FinFET

Region	Material	Mesh size
Substrate	Silicon	0.005
Gates(Tgate/Bgate)	Al	0.001
Oxide	SiO ₂	0.0005
Source/Drain	Al	0.001
Spacers	Nitride	0.01

I_d - V_d characteristics curve for MOSFET is shown in figure 13. I_d - V_d characteristics curve is obtained at $1e20 \text{ cm}^{-3}$ acceptor concentration and $1e20 \text{ cm}^{-3}$ and V_g varies from 0.25 V to 1.25 V.

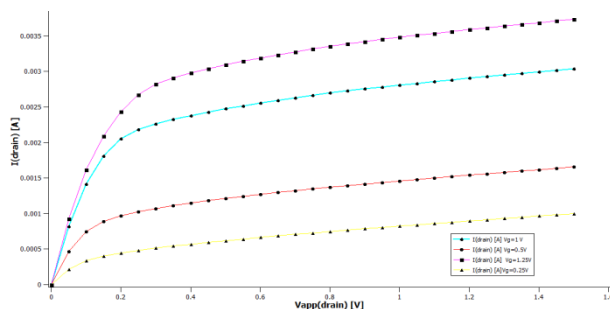


Figure 13: Output Characteristics (I_d - V_d) of MOSFET

The Id-Vd charcateristics of TFET is shown in figure 14.

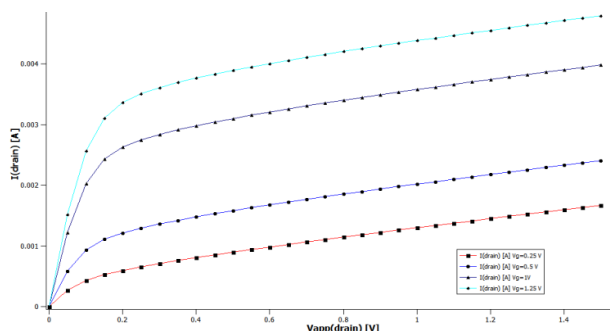


Figure 14: Output characteristics of TFET

To obtain the output characteristics curve for FinFET gate voltage is varied between 0.25 to 1.25 V and concentration of donor and acceptor ions is $7e20 \text{ cm}^{-3}$ and $1e16 \text{ cm}^{-3}$ respectively. Output characteristics curve for finFET is shown in figure 15

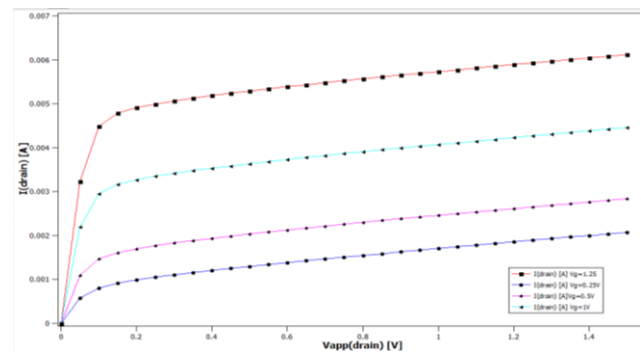


Figure15 Output Characteristics (I_d - V_d) of FinFET

5.4.2 Impact of Doping

The effect of impurities of source/drain of reversed type is observed by simulating the structure at different doping concentrations. It has been observed that drain current increases as concentration of ions in channel decreases. Figure 16 illustrates the MOSFET I_d - V_d characteristics at different acceptor concentration while keeping the donor concentration constant at $7 \times 10^{20} \text{ cm}^{-3}$. Drain current is 4.072 mA for lowest acceptor concentration i.e. $1 \times 10^{16} \text{ cm}^{-3}$.

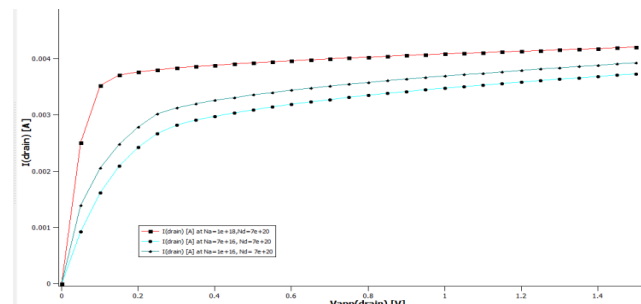


Figure16 MosFET at Different Acceptor Concentration

Id-Vd characteristics of TFET at different acceptor concentration and distinct donor concentration are demonstrated in Figure 17. It has been observed that drain current is max at lower acceptor concentration i.e. $1 \times 10^{16} \text{ cm}^{-3}$. The drain current is 4.05 mA at lower acceptor concentration

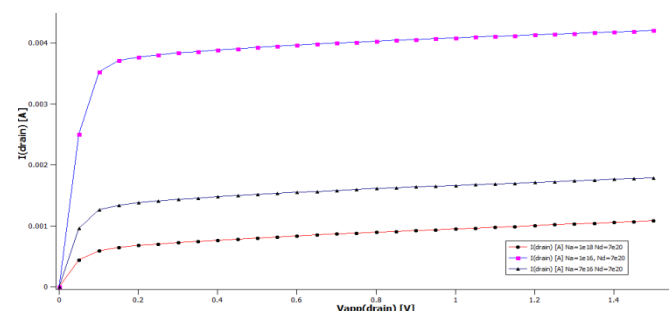


Figure 17: TFET at Different Acceptor Concentrations

Id-Vd characteristics of FinFET at different acceptor concentration and distinct donor concentration are demonstrated in figure 18. It has been observed that drain current is max at lower acceptor concentration i.e $1 \times 10^{16} \text{ cm}^{-3}$.

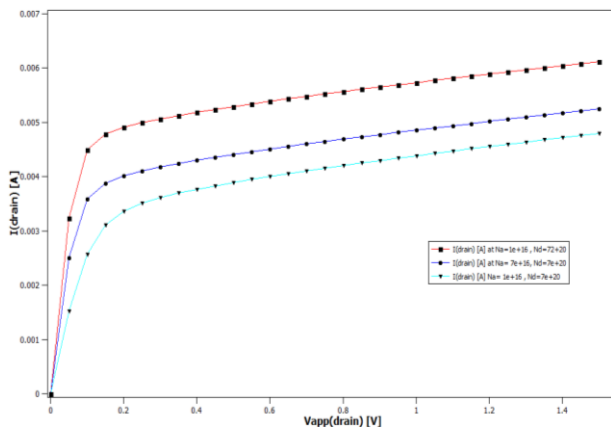


Figure 18: FinFET at different concentration

VI. CONCLUSION

Various FET structures had been discussed and reviewed in paper. The comparative study of conventional MOSFET structure with TFET and FinFET has been done. In order to get better knowledge of recent trends in FET structure, the circuit problems, fabrication and challenges had been discussed in the paper. In this, various FET structures has been compared at different doping concentration at channel length of 22nm. It is observed that FinFET possesses higher Ion current and drain current is max at lower acceptor concentration.

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