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Design and Analysis of Low Power 4T Sense Amplifier with Capacitive Offset Correction

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Abstract*: In this paper Sense Amplifier is analyzed the basic and fundamental operational block in the Static Random Access Memory. The function of the sense amplifier is to amplify the small signal bit line voltages into high voltages. In the existing literature survey, there are many methods available for designing the sense amplifier. In this paper, the cross-coupled sense amplifier is modified into a 4T based sense amplifier. The proposed scheme also developed for capacitive offset correction based sense amplifier. The existing and proposed designs of SA are briefly examined in this paper. The proposed design is implemented in the linear predictive technology model. The parameters like power and energy. The proposed scheme shows the better results compared to the existing method.

***Keywords* : Sense Amplifier, Mismatch, Read Write operation, Capacitive offset correction, Cross-Coupled, Power, Energy.**

I. INTRODUCTION

In today's computer technology, the SRAMs are most widely used cache memory. So the designs of SRAM consist of high speed and lower power consumption during read and write operational cycles. The entire speed and power were significantly affected the memory and its peripheral circuits. Sense amplifier is one of the important peripherals in the SRAM memory [1]. Fig. 1 shows the schematic of the single column SRAM. During the read operation of the SRAM, the sense amplifier circuit is operated to sense the input bit-line voltage differences. It produces the full rail voltage swing at the output terminal [2]. In case of computing or waiting for the full swing voltage level, the memory assumed as 1 or 0. Thus increasing its reading speed [3]. Developing trends in the scaling technology and increasing the attached cells, the capacitance bit line voltage is raised. Hence, the VLSA did not maintain their performance characteristics when the value of the capacitance is increased [4].

There are a lot design methods available for Sense amplifiers. The current mode SA was developed by [5] and its includes the overcoming procedures for imperfections. Theses imperfections are incorporated with the conveyers.

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R. D. Chandankhede et al 2014 [6] presented a novel Sense Amplifier (SA) circuit. This circuit is applicable to l KB SRAM. The sense amplifier is developed based on the current controlled mechanism as well as decoupled latching approach. The available voltage and ground discharging voltage are less than the Vdd. It is one of the improvement over the current controlled latch SA in terms of power consumption and performance. On the other hand, the nMOS depended SA is designed by [7]. This approach is used for high speed SRAM sensing. Likewise, the pMOS depended SA was presented by [8]. They are operating in a pulsed mode for single end SRAM with small Vdd supply.

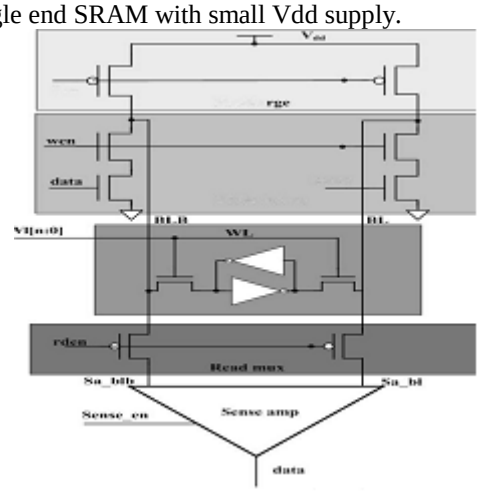

Fig. 1. Basic schematic of one column for small signal memory array using 6T cell [1]

The novel design of low power and high speed CSA was presented by [9]. In this method, the bit-line differential current is maintained by body bias of the transistor. The low offset scheme of sense amplifier was introduced by [10]. It also has the capability to work on the SRAM applications. This offset correction mechanism is further developed by [11]. The author presented the new technique for the cancelling of capacitive offset in the current mode SA. This technique involves the cancellation of capacitive offset and replica timing which enhance the operating speed. It is also suitable for the smallest Sense Amplifier area. Another novelty approach was introduced by [12] and it is known as LSTP-C2SA. Without creating any SRAM cell instability, the Dual rail SRAM's supply is decreased. It was activated by LSTP-C2SA.

Fig. 2 illustrates the brief overview of the SRAM column architecture with different offset mechanisms. The SRAM column elements are generated the offset superposition and VOS,tot is formed by combining the offset and SA voltages (VOS, SA) . The reading data is sensed by the differential signals which are originated from the memory cell. The memory cell has the current which is denoted as Icell.

The unpredictability of the SA enable timing is caused by the different factors such as non-uniform capacitive coupling to the bit-line signals, distributed capacitive loading of the bit-lines and Icell variations. In addition to this, the performance ability of the cell current to produce the high bit-line voltage is decayed by the changes in the capacitive coupling in column wise loading, missed out column cells and discharging current. Due to this, a mismatching problem occurs in the memory cells. This can be joined with the column loading to produce the bit-line variations for a time period of tSet. These bit-line variations are transferred to the Sense Amplifier input-referred offset and also perform the addition of VOS, SA. Fig. 2 shows the easier form of the cross-coupled architecture when the bit-line attained the Sense Amplifier. This also donates the complete VOS,tot [13]. The sense amplifier creates the input referred offset which is defined as the superposition of dynamic and static offset sources.

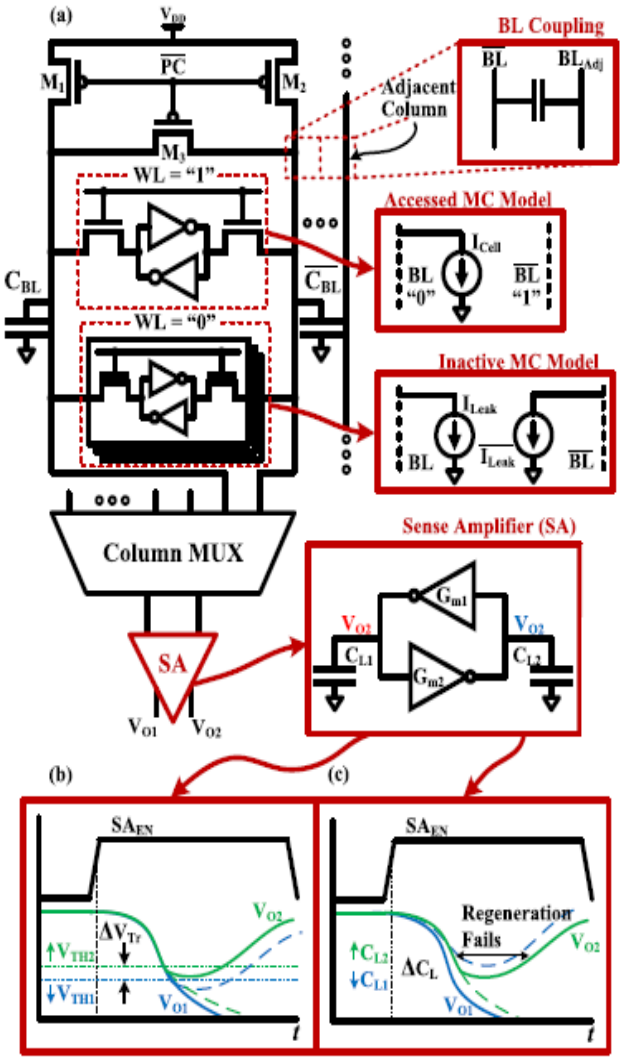

Fig. 2 (a) Offset contributions from the column of the single ended Sense Amplifier. Reading failures due to (b) static offset mismatch (c) dynamic CL mismatch [13].

In the cross-coupled sense amplifier, the mismatching condition occurs in the trip points (VTr) of the inverters. Because of this mismatching, the static offset can be made in the sense amplifier. This can be clearly expressed in the Fig. 2 (b). The reading failure is made when the trip points beginning the earlier changeover of the V02 compared to the V01. By increasing the size of the transistor, the trip point offsets are decreased. But it produces the huge amount area requirements as well as power consumption. It also produces one more shortcoming (i.e.) the capacitance value also increased for large device utilization. Those limitations have significantly reduced the SA latching speed. SA reading failure also caused by the dynamic CL mismatching. In this limitation, the differential discharge rate is modified by the CL. This made the quick discharging of the V01. When the value of the CL is too high, then the variations in the discharging rates of the voltages V01 and V02 cause the SA reading failure. To increase the performance of the better matching of the SA design, it must need exact layout design. This can be utilized in the additional calibration stages of the SA. By achieving the perfect timing of SA, a constant and dependable timing generation is very must. But the achievement is important for SRAM applications.

The above issues are generally overcome by introducing the two techniques. The primary approach designs the new sense amplifier configuration for trip points which is used for eliminating the both static and dynamic offset sources. This approach is done by a CSA with capacitive offset correction [13]. The secondary technique involves the generation of the process invariants. This can be done by column wise structure of the replica timing [13].

In this paper, the capacitive offset correction can be briefly analyzed and modification made in the cross-coupled inverter of the CSA. Hence, Section 2 represents the background methodology of the Sense amplifier timing analysis and its sensing schemes, Section 3 represents the proposed methodology of the COC, Section 4 represents the experimental results and finally Section 5 ends with the conclusion and future work.

II. BACKGROUND METHODOLOGY

A. Timing analysis of Conventional CSA

The conventional CSA is shown in the Fig. 3 (a) and its timing analysis is illustrated in the Fig. 3 (b). The conventional CSA is working as, when SAEN is '0', the transistor M6 is OFF state and disengages the latch. Normally, the transistor M6 is commonly referred as a tail current source. The SA output terminals (V01 and V02) separated from the path of the SRAM readout (DOUT, DOUT'). At the same time, the internal terminal nodes are shorted with one another and pre-charged to '1'. This internal node pre-charging makes the reduction in the dynamic offsets.

During the pre-charging process, the bit-line BL also pre-charged with the help of M1−3 pull up transistors. These pull-up transistors are placed in the column circuitry. After the pre-charging, the word-line WL is '1', which prompts the differential memory cell current (Icell). This Icell brings down the bit-line BL to the sense amplifier input. Hence, the overdrive voltages of the transistors M2,3 are proportionally modulated and is inserted into latch in the enabling time of the SA. This can be done by the different Icell. The conventional CSA has the differential overdrive voltage at the input terminal which is same as the Δ BL and is directly proportional to the Δ tSet magnitude.

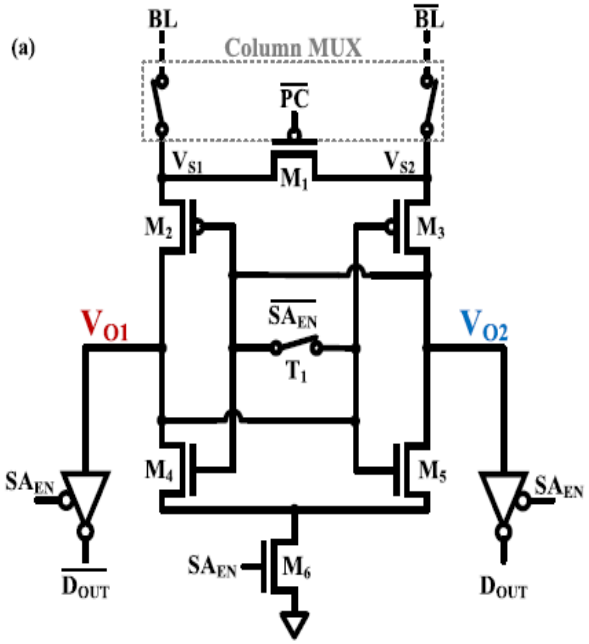

Fig. 3 (a) Conventional CSA diagram (a) schematic of simplified cross-coupled latch

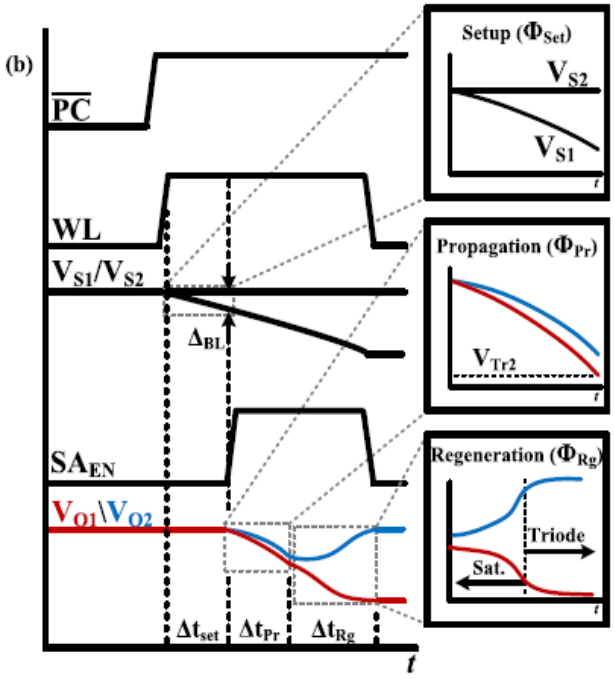

Fig. 3 (b) timing diagram

B. Sense amplifier with Capacitive offset correction

Fig. 4 (a) demonstrates the CSA with Capacitive Offset Correction (COC). The CSA-COC is similar to the conventional CSA which has the following supplementary components: (i) COC, (ii) M1,7,8 are considered as the local pre-charging circuitry, (iii) M9-14 are controlling switches for the 2 phase operation which is performed prior to the assertion of the word-line WL. At the initial phase of the capacitive offset correction, trip point storage (Δ Trs) accumulates the difference between the trip points (Δ VTr) of the inverter. In the secondary phase, the cross-coupled inverter latches are biased to its corresponding VTr. This is known as trip point bias (Δ Trb).

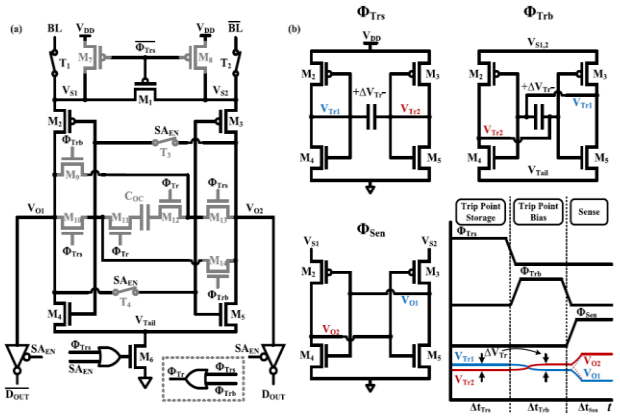

Fig. 4 (a) Schematic diagram for the CSACOC (b) timing diagram of CSACOC with different operational phases [14].

C. Basic Operation of CSACOC

The CSA-COC is analyzed in the presence of both dynamic (Gm, CL) and static (VTr) offset sources. They are extremely based on the inverter's trip points VTr. The presented architecture of the CSACOC reduces these offsets by means of productive storage of the difference in the inverter trip points (Δ VTr) which are trailed by the latch output re-biasing. These difference trip points (Δ VTr) are stored in the COC based cross-coupled inverter latch.

The dynamic offset of the CSA is significantly reduced by the reconfiguration of the COC and it is utilized in inverter biasing at corresponding VTr. The 2 phase operation and timing model of the CSACOC is clearly shown in the Fig. 4 (b). Let φ Trs and φ Trb are the two phases occurred in the accessing time of the row and it does not contain any RDᴛ timing overhead.

In the initial set-up phase (φ Trs), the latches presented in the inverter are detached from the cross-coupled state. They are moving into the diode-connected configuration. The CSACOC supply rails are associated with this set-up phase, so that the output nodes are considered from the trip points (VTr1,VTr2) of the inverters. Therefore, the shoot-through path is formed in between the diode connected devices and the supply rails. This causes the increased level of the power consumption of the CSACOC in the set-up phase. By introducing the optimal timing, this power consumption can be reduced. The amount of power is also saved when the lower bit-line BL discharging time. It also helps to cancel out the adding of shoot-through overhead in the CSA-COC.

The secondary phase of the CSACOC is propagation phase (φ Trb). In this phase, the inverters are moved with the short period of time. The capacitive offset correction is assumed as an equalizing capacitor which is used to bias the inverter latch inputs with their respective trip points VTr. In this phase, the latch outputs are not constrained because the left floating issues are occurring in the sources of the latch transistors. This makes the COC to simply locate the latch output nodes corresponding to its VTr without any over- constrain.

The final computational process of the propagation phase is assumed at the beginning of the third phase called sensing phase (φ Sen).

In the final phase (φ Sen), the nodes in the output terminals are biased at trip points VTr of the inverter latch. This is drastically deduced the offset. The COC is entirely detached (i.e.) transistors M9-13 are in OFF state and the latch (T3-4 are in ON state) is completely occupied in the φ Sen phase.

Phase's φ Trs and φ Trb are operated during the memory row address time and disengaging of the COC which are used to permit the CSACOC to increase the speed of the inverter latch. This speeding mechanism of the CSACOC is identical to the conventional CSA. In the φ Trb phase, this strong offset correction approach gives the process invariant which is biased to the all latch inverters. By enabling the local pre-charge circuitry in the correction mechanism, the dynamic offset is completely eliminated from the SA memory. Hence, V01 and V02 internal nodes are pre-charged to a known state which are prior to VTr1 and VTr2. But, there is no prior state of memory in the CSA-COC architecture.

D.CSACOC Timing Analysis

The simple linear model of the CSACOC and its timing analysis during the setup phase (φ Trs) are shown in the Fig. 5 (a) and (b). The circuit analysis is done in the set-up phase is identical to the approach which is used for measuring the trip points VTr. The latch inverter is made up of the MOS devices. These MOS devices are diode connected to the n-type MOS switches. The difference in the trip points (Δ VTr) is enhanced between the COC capacitors.

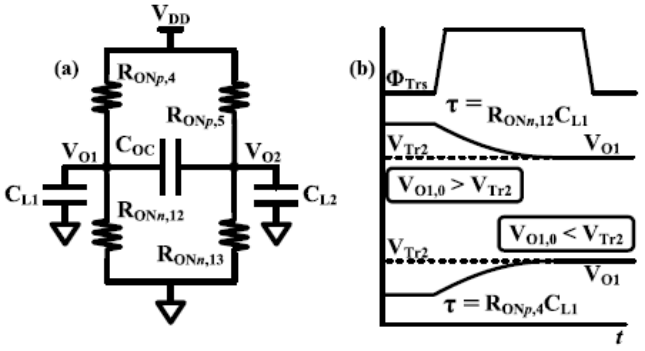

Fig. 5 (a) Simplified circuit and (b) timing analysis of the CSACOC in the set-up (φ Trs) phase.

E. Sensing Schemes of the Sense Amplifier

The sense amplifier's sensing performance is improved by introducing the three different schemes. They are AC Coupled sensing scheme, domino sensing scheme and switching pMOS sense amplifier. These schemes are used to sense the data based on the single bit line [15].

Domino Sensing Scheme – Fig. 6 shows the representation of the domino based sensing scheme. In this scheme, the local read bit-line (LBL) is tied to the dynamic p-type MOS transistor. If sensing bit φ is low, the pMOS transistor is switched ON and Z is charged. This causes the switch ON the next pMOS transistor. This enabling the GBL to the pre-charged state. The domino scheme requires a full swing of the local read bit-line. Due to this requirement, the dynamic power consumption based on the RBL capacitance is increased and at the same time it reduces the performance.

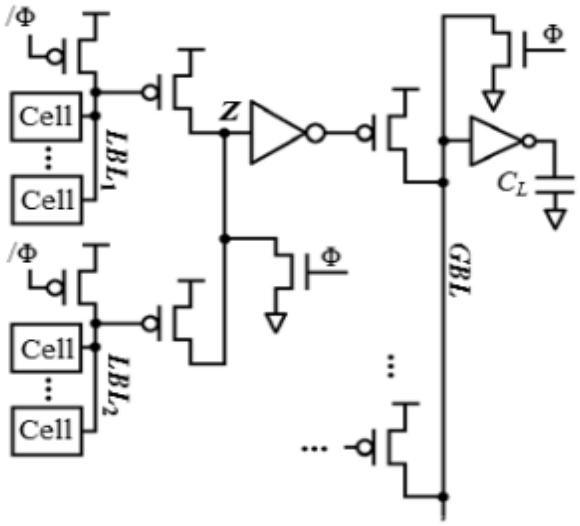

Fig. 6 Domino Sensing Scheme

Pseudo-differential Sensing Scheme – Fig. 7 demonstrates the pseudo-differential sensing scheme structure. The voltage sense amplifier based on the latch type with the reference input is utilized for multiple sensing. This scheme is mainly employed for the single ended SRAM circuits. The main objective of the sense amplifier is to amplify the small bit line voltages into higher level. In domino logic, this was done by introducing the full swing RBL. But it is needed in the pseudo-differential scheme for obtaining the better performance. Instead of RBL requirement, it needs an additional processing phase for acquiring the static and dynamic offset sources. It involves the additional strobe signal requirements to accomplish the above offset correction. This scheme requires an additional large amount of coupling capacitors which limits usage of metal and increases the area overhead. These are performed for discarding the potential offsets in the output nodes and BL.

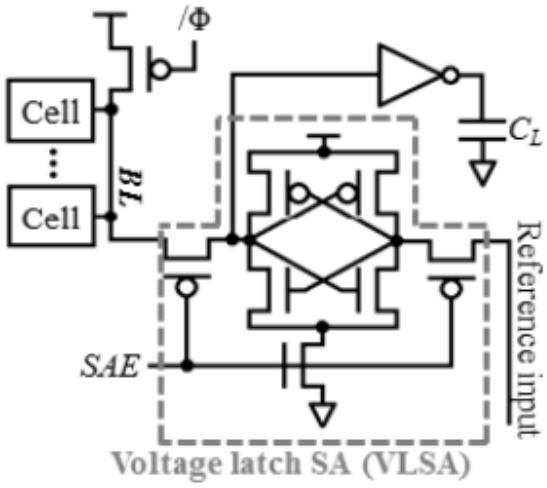

Fig. 7 Pseudo-differential sensing scheme

AC-Coupled Sensing Scheme – The AC-Couples sensing scheme of the sense amplifier are illustrated in the Fig. 8. The scheme employed in the one bank (i.e.) two-sub banks. The coupling capacitor of this scheme is denoted as Cin. ACSA includes the different processing elements such as CMOS inverter INVA which is made from one pmos transistor MAMP and two nmos transistor MD, and MEN), output charging p-type MOS transistor (M0) and equalizing p-type MOS transistor (MEQ). During the read operation, the inverter is activated by the MEN. This is performed for minimizing the static power consumption.It is operated in two phases such as precharge (φ =1) and evaluation (φ =0) to perform the sensing scheme.

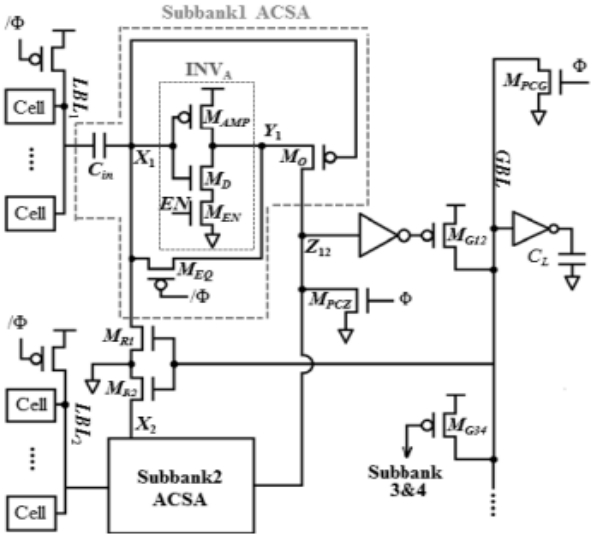

Fig. 8 AC coupled Sensing Scheme

III. PROPOSED METHODOLOGY

In memory design, the sense amplifier is the vital circuit to amplify the small differential bit lines into logically high signals. This is also applicable to the long interconnection signal reception which has the huge amount of CL signals as well as RC delay. Therefore, the sense amplifier is merged with the differential logic circuits to enhance the complexity of the differential logic circuits. This is also used for minimizing the delay period of the logic circuits.

For large SRAMs in CMOS technology, the designing of the sensing amplifier is a complex as well as challenging issue. This is due to the large SRAMs includes the N number of lengthy bit-lines which loads the memory cell based on the huge capacitive load CL. This produces the addition signal delay in the memory reading path.

The most important functionality of the sense amplifier is to sense and amplify the input data signals. These signals are transferred through the cells of the memory to the bit-lines. Below the supply voltage, the fast sensing of correct data signals is more complex. So, every time the bit-lines are loaded into the huge number of memory cells. In other words, the loading process of the BL is entirely high. Hence, the delay of sensing the correct data is one of the drawbacks in the reading access time of the SRAM. The most widely used cross-coupled SA is demonstrated in the Fig. 9. The complementary structure of cross-coupled inverter is made from the two pull-up pmos transistors (MP1 and MP2) and two pull-down nmos transistors (MN1 and MN2). The cross-coupled SA has the speed and loading characteristics which are based on the discharging conductivity and cross-coupled capacitance values. The conductivity is inversely proportional to the capacity (i.e.) it produces the larger conductivity for minimum capacity.

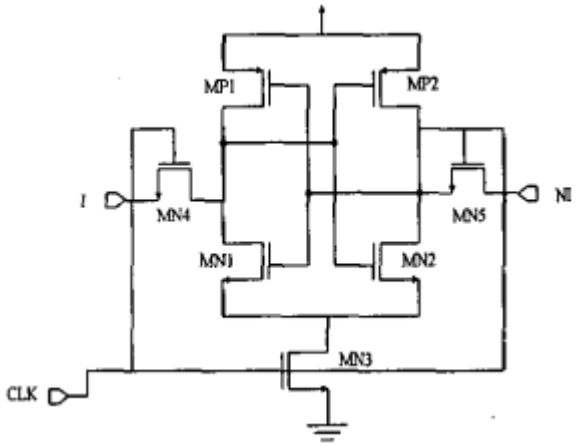

Fig. 9 Commonly Cross-Coupled Sense amplifier [16]

In Fig. 9, there are two cross coupled inverter is connected to perform the sensing scheme. This cross coupled inverter is replaced by two transistors. The proposed cross coupled sense amplifier is shown in Fig. 10.

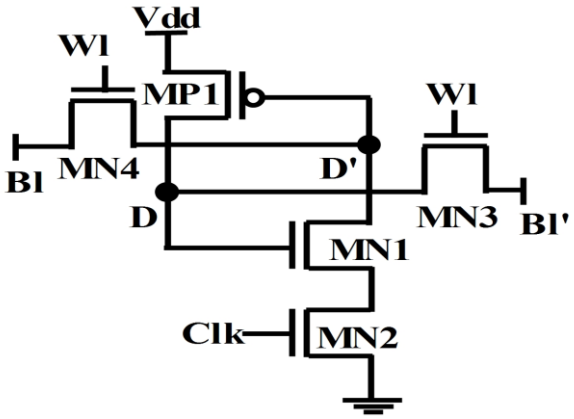

Fig. 10 Proposed Cross-Coupled Sense amplifier

The cross-coupled inverter in the Fig. 9 consists the four transistors MP1, MP2, MN1 and MN2. These four transistors are replaced by two transistors MP1 and MN1 in the proposed design. When Wl is asserted, the transistors MN3 and MN4 are turned ON. It passes the bit-line voltages to output terminals D and D'. This proposed approach is also applied to the conventional SA and the capacitive offset correction based SA. These are illustrated in Fig. 11 and Fig. 12. The proposed approach contains less number of transistors compared to existing approach [14, 18-23].

IV. EXPERIMENTAL RESULTS

The overall implementation is held in the linear technology spice model. The conventional and existing capacitive offset correction sense amplifier is designed and analyzed. The parameters of both designs were tabulated in Table 1 and 2 respectively.

The parameter analysis of the proposed method is tabulated in the Table 3 and 4.

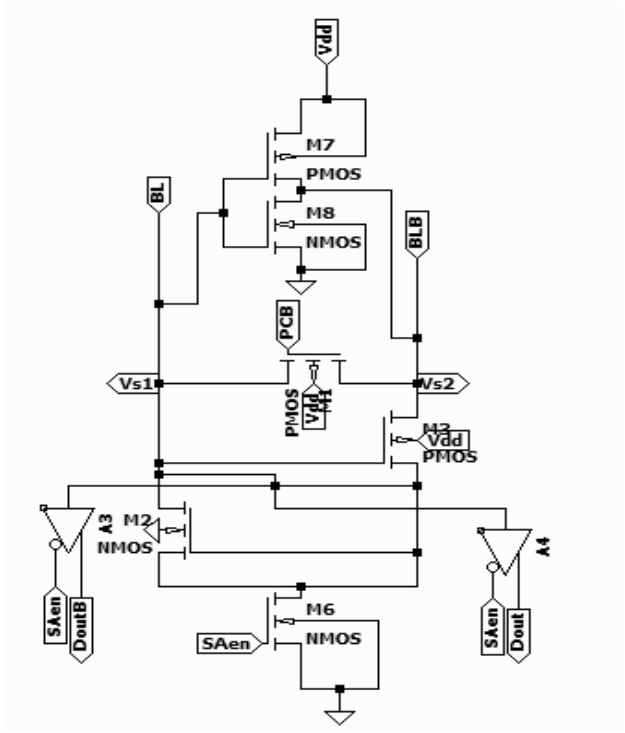

Fig. 11 Schematic view of the Conventional SA modified by Proposed SA

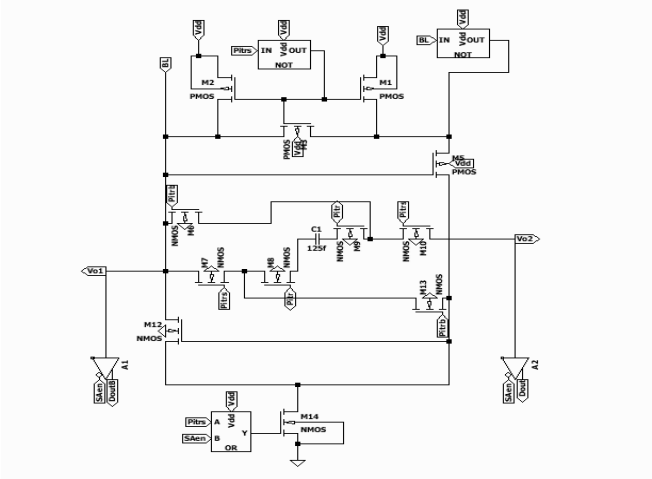

Fig. 12 Schematic view of the CSA-COC modified by Proposed SA

TABLE 1
Parameter Mesure of Csa

	At Vs1	At Vs2	At Dout	At Doutb
Vrms (V)	709.46 m	710.62 m	643.68 m	707m
Vavg (V)	505m	537.63 m	415.57 m	500.68m
Pavg (W)	464.04n	464.04n	15.471n	656.61p
Eavg (J)	4.1764 µ	4.1764 µ	139.24n	5.9095n
M1 (W/L)	0.68/0.12			
M2,3 (W/L)	2.72/0.12			
M4,5 (W/L)	1.36/0.12			
M6 (W/L)	2.72/0.12			
No. of T	06			

TABLE 2
Parameter Mesure of Csa -coc

	At Vs1	At Vs2	At Dout	At Doutb
Vrms (V)	502.83m	502.3m	444.96 m	445.27 m
Vavg (V)	345.71m	345.24 m	200.18 m	201.01 m
Pavg (W)	4.3035n	2.4123 n	16.501 µ	16.501 µ
Eavg (J)	86.07 µ	48.247 n	330.02 µ	330.02 µ
M1-5 (W/L)	2.72/0.12			
M6-14 (W/L)	1.36/0.12			
No. of T	14			

TABLE 3
Parameter Mesure of Proposed 4T Based Csa

	At Vs1	*At Vs2*	*At Dout*	*At Doutb*
Vrms (V)	709.46m	327.98 m	710.22 m	710.22 m
Vavg (V)	505m	197.76 m	504.85 m	504.85 m
Pavg (W)	137.01n	990.02 n	736.45 n	585.75f
Eavg (J)	1.3701µ	9.9002 µ	7.3645 µ	5.8575 p
No. of T	04			

TABLE 4
Parameter Mesure of Proposed 4T Based Csa-coc

	At Vs1	*At Vs2*	*At Dout*	*At Doutb*
Vrms (V)	709.46m	142.05 m	128.7m	710.3m
Vavg (V)	505m	74.672 m	17.801 m	505.02 m
Pavg (W)	686.13n	342.65 p	661.11 n	405.37 n
Eavg (J)	6.8613µ	3.4265 n	6.6111 µ	4.0537 µ
No. of T	12			

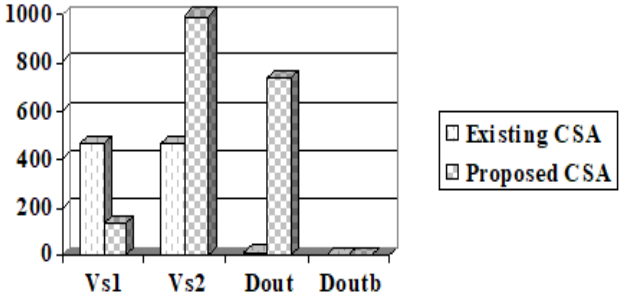

Fig. 13 Comparison of Existing and Proposed CSA at different nodes interms of power (nW)

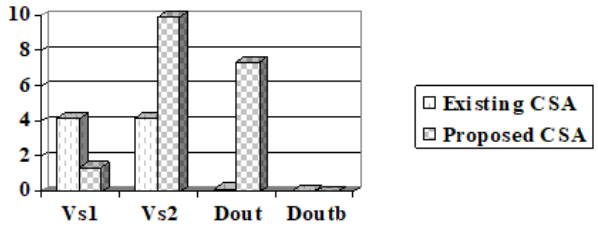

Fig. 14 Comparison of Existing and Proposed CSA at different nodes interms of Energy (µJ)

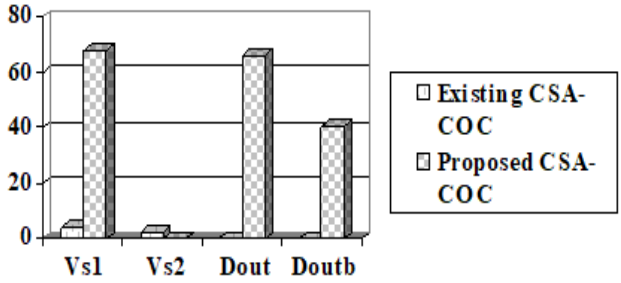

Fig. 15 Comparison of Existing and Proposed CSA-COC at different nodes interms of power (nW)

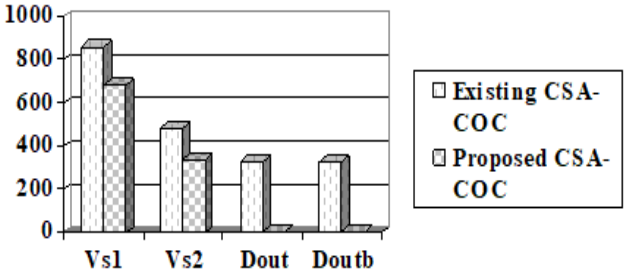

Fig. 16 Comparison of Existing and Proposed CSA-COC at different nodes interms of Energy (µJ)

Fig. 13 and Fig. 14 show the comparison of the existing and proposed CSA by measuring the power and energy at different output nodes such as Vs1, Vs2, Dout and Doutb. But it does not show better results in the conventional approach of SA. Fig. 15 and Fig. 16 show the comparison of the existing and proposed CSA-COC by measuring the power and energy at different output nodes. It shows the reduced level of energy when compared to the previous approach.

V. CONCLUSION

In this paper, an efficient low power scheme of sense amplifier is designed. The read and write operation of the SRAM is performed faster by implementing this sense amplifier scheme. The presented approach consists of less number of transistors. This causes the reduction power and energy in the different output nodes. The proposed SA will be developed to 32nm CMOS processor. It consumes less amount of parameter utilization when compared to the presented design.

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