International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9 Issue-7, May 2020

Recent Advancement in the Memristor Memory Development

Ravikumar K. I, Sukumar R

Abstract: ***Meritor is a newly-created tool and because of its nanometer scale and different electrical properties it has received much interest from advanced electronics designers since it was discovered. The memory capacity of a memrist is one of the most significant features. In this paper, about 50 papers on designing of memristor, optimization rules for reducing power, area for storing the data into memristor and implemented the full adders using memristor using the Pspice simulator. The paper ultimately addresses the complex study lapses and obstacles in constructing the memorial that will enable scholars and thinkers lead to more analysis.***

Keywords: memristor, optimization.

I. INTRODUCTION

The resistive memory of the Crossbar has recently gained tremendous publicity owing to its amazing high density and overall scaling. Many two terminals with nonlinear power-tension features (I−V) in the crossbar RRAm arrays were suggested in order to incorporate the crosstalk from the unwelcome sneak current into the memory device series via the neighboring read-and-write operating cells. [1]-[2].

PCM, MRAM, FERAM and RRAM are attracting a large volume of industry and education attention in a modern paradigm, while traditional flash records hit their limits. Excellent RRAM technologies are known to have huge potential for mass storage and integration, particularly its low energy usage, ready set-up, ready-to-sale deployment and high-speed running. [3]–[7].The RRAM has been gaining a large amount of competition as the next wave of memory technology [8-11] from Metal Oxide-based resistive switching. In existing CBRAM systems the desired self-rectification characteristics can be effectively combined with an amorphous (aSi) layer. ACOS-compatible and strongly non-linear is the aSi-based selector [14], [15]. The Cu / Al2O3/aSi / Ta structure providing strong nonlinearity in this study retains the high on / out ratios and stable low current activity even in complying with external law.

The components and the production methods used in this RRAM cell are entirely CMOS compliant with the peak production temperature of 150 ° C.

Revised Manuscript Received on May 30, 2020.
***** Correspondence Author
Ravikumar K. I*, Pursuing Ph.D., Jain University, JGI Global Campus, Bengaluru, Karnataka, India.
Sukumar R, Professor and Head of ECE , Jain University College of Engineering & Technology, JGI Global Campus, Bangalore, India

The memristor is a lightweight system (as seen on [16]), b) quick switching activity (in 10 ns [17, 18]) c) low tension programming specifications (around 1V programming voltages as referred to in [19]) and d) manufacturing methods compliant with CMOS relative to other NVM systems. Relative to other MRM (Resistive random access memory) there are specific advantages. The RRAM is combined with the SRAM cell in past works such as [20–23], but each configuration either contributes to substantial deterioration of the fundamental SRAM reading process or absorbs a huge amount of energy for the storage / restoration of data to / from RRAM as described further in depth in section 4. In our paper we give a new NV-SRAM 8T1R that is similar to a standard SRAM 6 T device with reading power, delay and noise tolerance. In turn, since only one RRAM cell is required for the off-time storage of SRAM data, energy used for processing RRAM data is reduced by more than 60% relative to the lowest energy density of previous RRAM NV-SRAM designs. In contrast, the energy consumption of the regeneration process decreased by around 70%.

II. BACKGROUND

A. Baseline 2-D FPGA

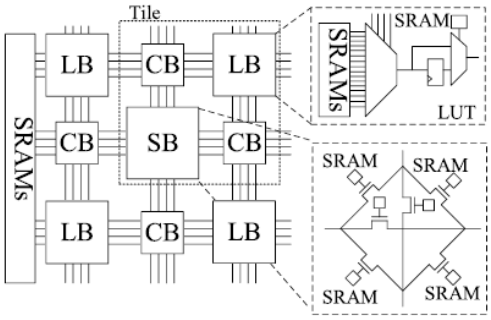


Fig. 1. Easy island-style FPGA architecture based on SRAM.

As seen in the photo. 1. This article is based on the standard 2-D FPGA-Island architecture[24]. It has many tiles. One SB, two CB and one LB per file consisting of various local routing schemes to route input signals to specific logical features (SLF) and to link BLE outputs to their inputs. For routing, the fig is linked to LBs. 2. Possible I / V modules that can be installed and disabled. The differences may be good, good, strong, unfavorable, negative, positive, and poor. Network CBs. Network CBs. CBs. CBs. The number of paths to LB is regulated by an architectural parameter Fc (the ratio of the input to output tracks of the LB and the width of the channel W). The national routing network comprises of independent 2-D SB linking channels.

B. RRAM

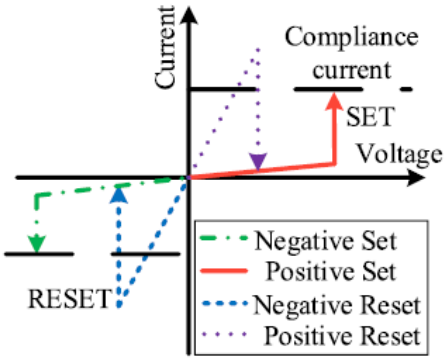


Fig. 2. Possible Install and Replace I / V configurations. The variations may also be good, good, positive, positive reset, null, optimistic, and poor.

The fundamental idea of the RRAM switching mechanism is that an isolating dielectric can be conducted through a filament or a path. With the application of the appropriate voltage the RRAM can reversibly be switched from HRS (fragmented filament) to LRS (reformed filament).

Many possibilities are shown in the figure of the fixed and reset curves. 2. The lower voltages work as a reset for unipolar switching and the higher Voltage works in the same direction as fixed, while negative reset (eightways) and positive reset (eighwise) for bipolar switching only can be changed [25] [26]. The optimistic package, optimistic reset unipolar flipping activity is used in this NVFPGA formulation because of the compose scheme employed in our original NVFPGA to remove sneaks.

C. Access Device

The sneak route issue arising in passive CBs, SBs and local interconnections is a big obstacle to incorporate the RRAM cell as switches into the FPGA. Diode is used as the tool of access to escape the sneak-path and to reach high density since it is simple to access[27]-[30]. It can also provide large ON / OFF ratios and high driven current.In the case of a recent Cu-ion movement in the Cu-containing MIEC material, for example, International Business Machines Corporation has demonstrated a high density (> 50 MA / cm2) and strong ON / OFF ratios (To). The stacking of FPGA CMOS RRAM and diode will minimize the FPGA region and delay significantly, thus increasing the performance of FPGA significantly.

D. Related Works

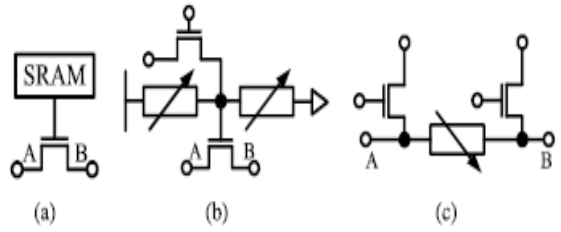


Fig. 3. (a) Conventional SRAM storage for FPGAs setup (SRAM). (b) Non-violatile FPGAs (1T2R) Storage Configuring Feature. c) Non-volatile transistor and SRAM (2T1R or 1R) replacement storage part.

As Fig indicates. 3(a), the regular SRAM-based FPGA configures a nMOS transfer through the SRAM cell. The NVFPGA-based RRAM will configure the nMOS switch with a similar configuration as shown in Fig. (b). 3(b). A popular NVFPGA integration scheme based on RRAM is shown in the figure. 3(c) replacing SRAM as well as the nMOS transition in complete. Yet there are distinct shortcomings in both RRAM design methods that hinder execution of the NVFPGA. The 1T2R architecture shown in the chart. 3(b) has been stated to have the advantages of instantaneous turn-on and zero standby turn in the[31]–10] substitution of traditional SRAM cell with RRAM-based capacity. Unfortunately, the durability issue is weak and limits its usage in FPGAs. The poor efficiency of RRAM cells with VDD bias stress in action is the explanation for the weak retention. The high active leakage capacity due to the lack of high OFF resistance in RRAM cells is another concern. In comparison, the vth reduction of the nMOS switches dramatically lowers the FPGA's rpm. The nMOS switches may then be over-driven to decrease the ON resistance, which impairs the 1T2R element's efficiency and active leak strength. Fig. displays the 2T1R (1R) method. To substitute the NMOS switch with the SRAM cell for high speed, distance, 3(c) was suggested. The Vth reduction on the transistor programming therefore reduces the write current dramatically. More significantly, due to the significant leakage current in the sneak track it suffers from substantial low writing efficiency and high write capacity. For eg, the RRAM cell RNW programming between Fig N and W nodes. 4(a) The N potential is at Vset and Vresets (where the RRAM setting and reset voltages are Vset and Vreset) and the W node potential is the field. 4(a) If RNW, RSN and RSW are respectively situated at HRS, LRS, and LRS, the majority current moves through RSN and RSW. This contributes to an incredibly large leakage current as the resistance of RRAM cells in HRS and LRS varies from other orders. Consequently, RNW can not have sufficiently current to adjust. Writing problems will make the value of writing bad. As Fig indicates. The capacity for RNW and for RSW is about the same while rnw, rsn and rsw are in high, small and weak states respectively. This allows for the transfer of both RNW and RSW.

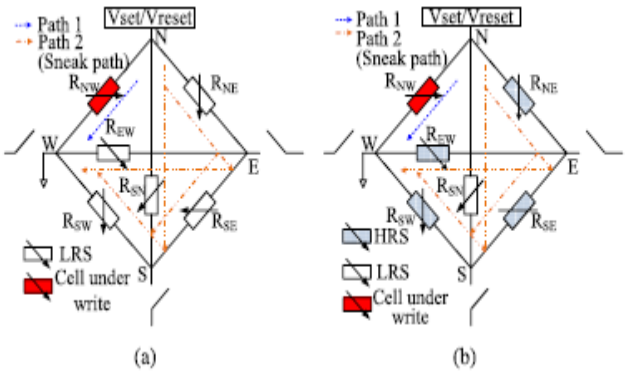


Fig. 4. (a) a strong current problem of leakage and (b) a problem of writing disruption in standard non-volatile SP dependent on RRAM. The en-dash lines are the way

RRAM cells are designed, and the stealth routes are the dashed-dotted patterns.

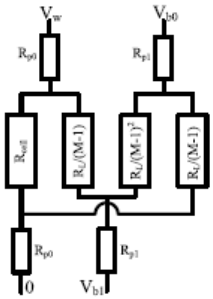


Fig. 5. The diodless crossbar collection identical circuit. Rcell is the programmable RRAM cell resistance, RL is the RRAM cell resistance in LRS, M is the array number, Rp0 is the trigger, wire, and so on, Rp1 is an input parasite resistance that is Rp0/(M−1) for a V/2 orV/3 written scheme, and Vw is the writing voltage, and Vb0 and Vb1 are the biased voltages.

While un-selected devices may minimize writing interference by half the (V/2) or by one-third(V/3) voltage, the flow rate is still extreme for the quality of the configuration data [40]. As seen in the diagram, the equal chain. 5 The sneak direction can be called equal to the programming cell, while unselected RRAM cells are at LRS. The parallel tension between VW and ground voltage is about 2(RL+ Rp0)/(M − 1), for example, when the V/2 Scheme is used. The remainder of the current is then oriented towards the pathways of the escape, and the parasite resistance Rp0 will overcome the equal resistance between Vw and the planet. Increasing VW to account for a decrease in write voltage may contribute to high risk of RRAM failure as Rcell voltage may be overly wide while the majority of cells are not chosen. In addition, high write disturbances can influence the unselected cells because they are partial to half the write voltage. The structure 1D1R or 1T1R will reduce the current from a sneak direction. Yet the FPGA routing route can not combine diode and transistor. If not, the voltage drop and the delay will increase. The implementation of non-linearity on the RRAM cell or the incorporation of a non-linear selector in series will minimize the flow rate and voltage. However, during FPGA activity the capacity for the ON RRAM cell must be negligible. Therefore, owing to the non-linearity that goes against a weak ON resistance to decrease the RC latency of contact in FPGAs, the ON resistance may be considerably high.

III. OSCILLATORY NEURAL NETWORKS

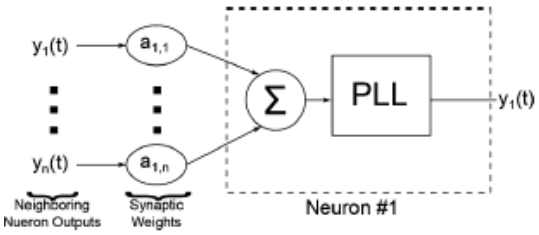


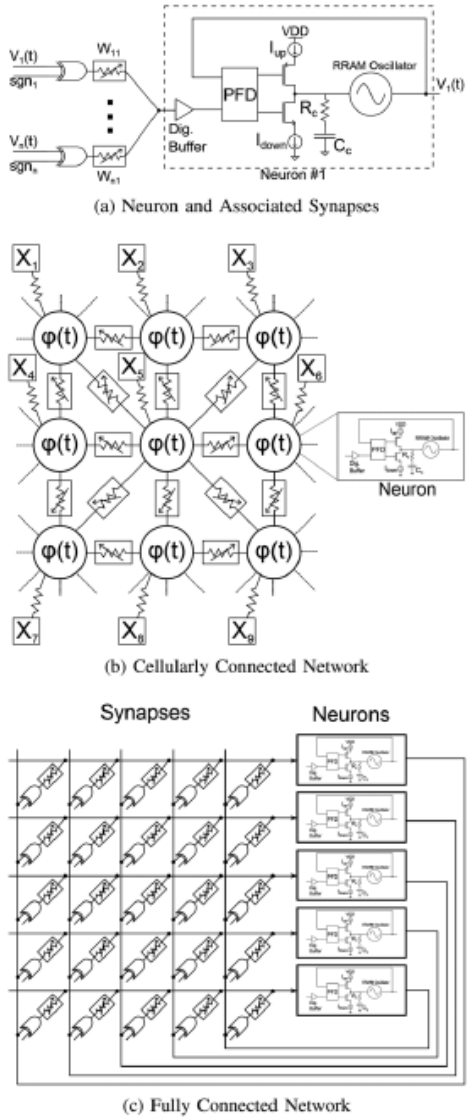
Fig. 6. One cell with an ONN logical model. The data is processed in the device as the output signals process of every PLL.

The Hoppensteadt and Izhikevich in [34] suggested oscillator neural networks (ONNs) consisting of mixed phase-locked loops (PLLs). In this ONN style, a PLL is the "neuron" in which the status of the system is integrated and saved while connections act as "synapses" or the weighted influence on another neuron. In the figure you can see a mathematical representation of an ONN node. 6. In [34] it was seen that the neurons synchronize with the same frequency in this network, and that their relative phases correspond to the network sequence. There have been several ONNs suggested and tested, but a flexible and reprogrammable mix of design and technology was not yet proposed. In a laser device, for example, neurons and holographic interconnections are suggested and interpreted as synapses[35], but major problems remain until such a method, including the creation of holographic interconnections, may be accomplished. A framework has been suggested and tested in [36] for a more feasible implementation. This device uses neurons and variable electronic links between MEMS-based oscillators. While there is technology for the design of such devices, no clear proof exists that such a device will calculate area and power through mechanical oscillator constraints.

A concept was developed and designed in [37] utilizing more conventional circuit components. The neurons in this network are built in a variable impedance by the van der pol oscillators. The framework of examples in this paper comprises of distinct components and the requirement for active analog circuits to provide the requisite negative impedances will be especially difficult to pass them to a deeply scaled, effectively scalable CMOS Circuit. The recently designed and built in ONNs based on the spin torque oscillators (STO)[38], which are capable of well scaling in terms of area and power. The only systems seen so far can not be reprogrammed because the link intensity is dependent on the physical distance between the oscillators. STOs have always a voltage drop in the mV range that makes it very difficult to build device circuits.

The neurons are seen by RRAM-based oscillators that are able to profoundly scale the region and power when working with CMOS circuits at voltages quickly. The actual RRAM components of the synaptic connections thus amount in region and power similarly. In the Figure there is a single neuron with its synaptic connections. 7(a), whereas in Fig some neurons are seen in two separate setups. (c) and (b) of 7(b). Synaptic connections inside an ONN involve analog programming, and therefore a DAC for each individual weight which is unfeasible as far as power and area scaling are concerned will be needed in a pure CMOS implementation. A CMOS VCO intended to deal with the RRAM oscillator's frequency and region scaling will be so often that it would need higher voltage (and thus more space) digital circuits. In this design the analog components are handled by RRAM machines, as opposed to the CMOS-only implementation, such that the remaining CMOS circuits are predominantly digital and can therefore take maximum advantage of method scaling.

Such RRAM systems are described in the following parts which include an overview to the physics that makes them ideally suitable.



(a) Neuron and Associated Synapses

(b) Cellularly Connected Network

(c) Fully Connected Network

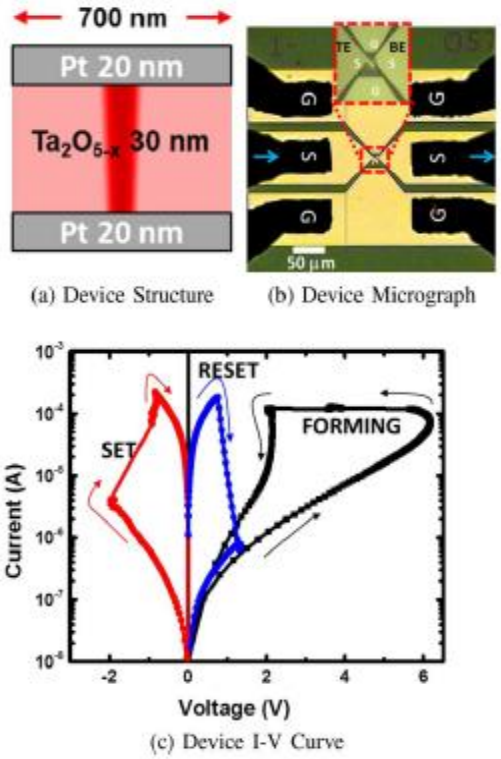
Fig. 7. ONN based on RRAM. (a) The synaptic links of a specific neuron. The stage is the network condition and the power values are the synaptic weight values. (b) Sample configuration of neurons in a system of mobile communication. The specifics of the neurons and synapses are omitted for connectivity. Display device inputs. (c) A full-linked sequence sample neuron setup. To achieve high synapse density, a crossbar array is used.

Bipolar flipping functionality tools. The method of switching is based on the growth / dissolution of leading filaments on the oxide layer. The model also catches the RRAM preservation property and the temperature dynamics in addition to the dc and pulsed I-V characteristics. Experimental knowledge from IMEC RRAM HfOx-based systems calibrates the software parameters and system variants. In Verilog A, the concept was introduced and can quickly be modified for circuit level research into the SPICE simulator. As case studies, we demonstrate implementations for the1-transistor1-resistor array programming scheme architecture as well as the 1-selector 1-resistor megabit-level configuration space exploration framework.

This segment explores the mechanics of resistive switching devices and how RRAM can be used to shape a synaptic function of several different rates.

A.RRAM Device Physics

Substochiometric metal oxides (TMOs) sandwiched between two metal electrodes can be used in resistive switching. We use a crossbar cell of Pt (20 nm)/TaO (20 nm)/Ta (5 nm)/Pt (15 nm), to illustrate the experiments in this article, as seen in Figure 2. 8(a) and (b), respectively. To act as a memory unit, these leaky metal insulators (MIMs) must go through a special mechanism known as the formation. Forming is a dielectric decomposition mechanism that contributes to the creation of a conductive filament. Such conductive filaments are considered by their positive charge to be agglomerated oxygen vacancies) formed because of high temperatures in the area and fields involved with the cycle of formation [39]–[41]. The system resistance varies from an incredibly high resistance to a lower resistance at the end of the shaping cycle. The video. 8(c) shows the black dc I-V shaping phase gradient. The cycle of forming is considered to be initiated by electronic localization that triggers the movement of oxygen vacancies electro-thermal[42].



(a) Device Structure (b) Device Micrograph

(c) Device I-V Curve

Fig. 8. RRAM computer designed with I-V properties for experimental demonstration. (a) a system diagram made. (b)

A research interface computer micrograph. (c) Measured I-V unit curves shaping and subject to

IV. METAL-OXIDE RRAM DEVICES

processes such as SET and RESET.

A reversed field may alter the resistance of the shaped structure, resulting in a "rupture" or "void" inside the filament. The cause for this breakup was a mixture of oxygen deficiency and oxygen depletion on the ground[40], [19], [43]–[45].

Such a filament rupture is associated with a transition in the unit resistance from a low resistance (LRS) to a high resistance (HRS) level. During transformations of the HRS LRS (known as SET) and LRS HRS (known as RESET), the voltage of the various polarities can be applied as seen in Fig I-V curves. 5(c). 8(c). The LRS values and the HRS values are the powerful functions of maximal strength dissipated during the shaping phase in the filament length. It should also be remembered that after creation, the devices stay in the Hours and then SET and RESET are identical to previous research. A higher distributed strength contributes to a wider filament [43] and [44] and thus a lower LRS rating. The average enforcement current during the development phase should be restricted to this point. Each SET change needs consistent compliance with full current to guarantee that the LRS can be repeatable. If the system is self-compliant [46], this need is prevented.

B. RRAM Synapse: Multi-Level Cell Operation

The analog weighting of signals from each neuron is provided by an ONN, as described in SectionII. Thanks to its capacity for multi-level service, RRAM devices may well fulfill this necessity. The core principle behind the multi-level (MLC) RRAM procedure is the adjustment of the filament configuration by modifying the full power discharge by the system during SET and RESET cycles. Zhao et al. [47] stated that a device of various pulse amplitudes may be used for the synaptic weighting process. This allows the system to lie on multiple resistance thresholds while the transfer takes place.

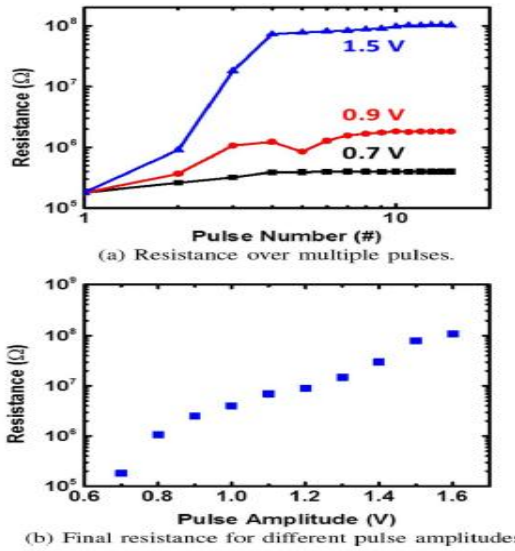


Fig. 9. Show of a RRAM device's MLC features. (a) the device's tolerance to multiple amplitude pulses. The systems are designed to minimize volatility using a pulse train technique. (b) Last resistance programming following pulse train wave amplitude training.

In the video. 9(a) a common pulse amplitude dependency of the system by three separate pule amplitudes is shown. We submit the device to a train of 15 pulses of the same pulsation duration (100 ns) for this experiment. A pulse train is used to reduce finishing value volatility as stated in [26] instead of a single pulse. In the first two or three pulses the unit resistance shifts and stabilizes to an almost constant value. Thermally-activated and field-accelerated the process of this programming. Increasing voltage produces a mixture of electric-temperature fields that eliminates oxygen vacancies from filaments, allowing the resistance of the system to increase. However, when all the oxygen vacancies are removed from the filament for the temperature-field combination, this procedure no longer changes device resistance. The video. 9(b) indicates that with various pulse amplitudes, the fine grained regulation of the unit resistance is feasible. For this experiment, the resistance of the system used can be regulated by three magnitude instructions, from 150k to 150M. This resistance regulation allows the system to be used in the ONN as a synaptic weight.

C.Switching Mechanism of Al/Ni/Solution-Based AlOx/Pt RRAM

The RS modeling with appropriate curves, shown in Figure 10a, is used for the investigation of the driving meechanism with standard bipolar RS output shown with the Al / Ni / solution-based AlOx / Pt RRAM system. Figure 10a demonstrates that the prevailing conduction system for 250 annealed devices displays room charging minimal current (SCLC). The findings are optimistic and negative, in double logarithmic maps, for I-V zones. Since of the nearly equivalent values of CC and RESET present, a significant variance between SET and RESET may be found. Ohmic piping (I / V) in low voltage (51,52) is found with the currents. The OFF-state direction indicates a change towards approx. 2.0, in line with the Child's square rule at higher bias voltages[53,54]. The slope increased to about 8.7 again in line with the SCLC process by further rising the voltage applied[53–56].

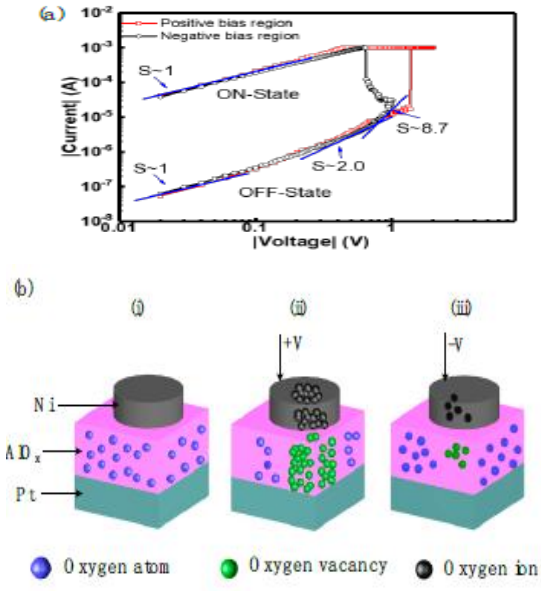


Fig 10. (a) I-V configuration of Al / Ni / AlOx / Pt System based on RRAM with SCLC conductivity. (b) diagrams showing the initial state RRAM Al / Ni / AlOx / Pt switching cycle, (ii) ON and (ii) OFF Figure 10. Chart 2. Chart 2. Form 10. Table 10. (a) I-V ideal for RRAM solutions Al / Ni / AlOx / Pt showing SCLC conduction. (b) diagrams showing the Al / Ni / AlOx / Pt RRAM flipping mechanism at the initial level, (ii) at the ON and (iii) at the OFF zone, respectively;

In the SET / RESET period [54–56.57,58], it is well-known that the bipolar RS of all RRAM units at annealing temperatures is related to conducting filament (CF) production and fractionation in association with oxygen vacancies. This process is represented schematically by ON and OFF states and is defined by Figure 5b as the switchable feature of these devices. The creation and breaking process of CF is related to the distribution of oxygen ions and oxygen vacancies in the TE and RS layers. Figure 5b(i) shows the oxygen atoms present in the thin film even without the applied voltage in the initial state of RRAM devices. To order to convert the yellow oxygen ions into the TE, the electrons are stuck with oxygen atoms on AlOx thin foil[59-61] with a positive voltage to the ni electrode during the SET process.

The oxygen vacancies are present in the AlOx thin film and are essential to CF. As shown in Figure 10b, in the ON state of RRAM method, this stage of development of the CF consisting of oxygen vacancies inside the AlOx thin film is named the transitional resistance state (HRS)[58]. In RESET operation, an electrical field effect of oxygen ions accumulated in the electrode drift on a thin AlOx layer, with the negative voltages applied to TE, decreases the oxygen vacancy density of the AlOx thin film. The motion regulates the breakdown of the CF[22] and the operation of the OFF structures (LRS to HRS).

Fabrication Process

Figure 11 demonstrating momentarily the phase flow of our RRAM cell between metal A (low metal) and metal B (high metal) stacks. Plug BE Touch consists first of dry andch, then void fill, TE rough masking dry etch et TE etch surface videos. Fig.12 displays the TEM RRAM interface diagram consisting of the lower electrode (Plug-BE), a resistive panel and a Top Electrode (TE) touch shape brush.

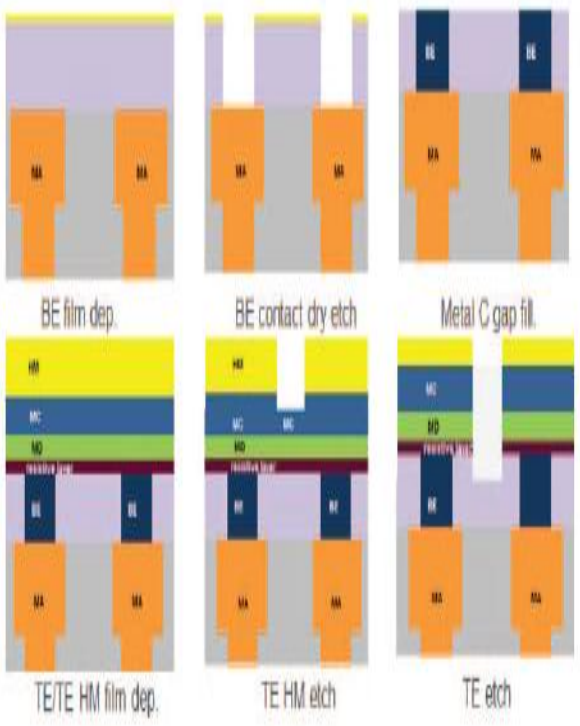


Fig.11. RRAM cell arrays flow.

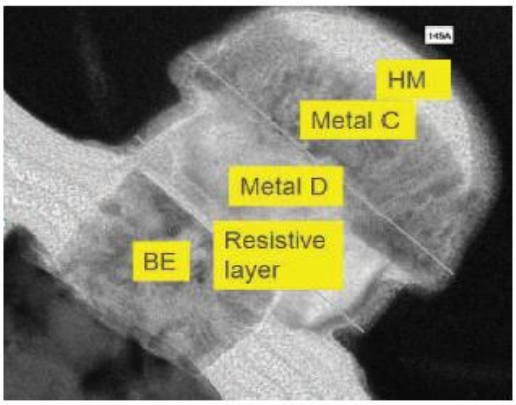


Fig.12. TEM image of the fabricated unit RRAM cell.

A. Issues

Thanks to the RRAM cell island design (super high transmission rate~97 percent), a variety of problems have been faced during the produce. Fig.13 demonstrates bad uniformity trends after TE hard-mask etch, where the wafer center CD is smaller than a boundary CD. Trends of bad uniformity This issue will affect the final uniformity of the RRAM cell and the unit performance.

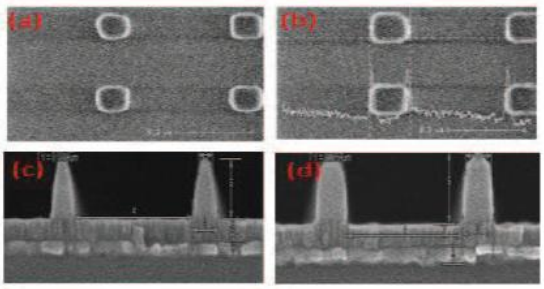
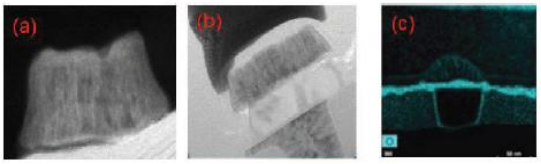


Fig.13. The pictures of a, b, and c, d are CDSEM pictures of top view and transversal electrons scanning images, respectively, post TE HM etch (a), c) wafer core, b) wafer edge and (c) wafer photos, respectively.



Picture.14. (a) BD dep TEM graphic. TE etch email. There is no sheet of metal D video. (b) TEM metal B trench graphic, which indicates metal B and TE are not related because of HM residue. (c) EDX check photo following TE etch, indicating TE oxidation.

Fig.13(a),(c) demonstrates the question of post-TE etch: (a) missing TE metal D issue; (c) HM oxide oxidation question. (b) indicates the TE / metal B trench etch contact point where the HM is placed. The loss of the RRAM signature is due to these complexities.

B. Solutions

TE HM etch method uses three layer scheme in which the first two stages split three layers; the third step is key etch with HM oxide; and the last step is a PR string. The second stage is three layer breaking through. In accordance with our step-by-step partial etch test the PR consumption of the first two phases is rapid, particularly in the wafer center region and may be due to HM mala uniformity as shown in Fig.15.

The irregular PR intake can arise from the small island pattern of RRAM and can be linked to the state of the etch chamber (60C). The first two measures also adjusted the temperature to 20, which is clearly increased in Fig.5. We conclude that the PR consumption is temperature-sensitive in our special design especially in the center region of the wafer. In addition, lowering the temperature of the etch chamber can decrease PR consumption and then enhance CD consistance.[41]-[52]

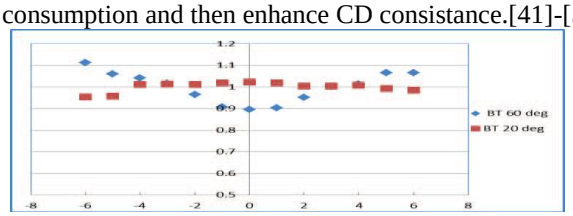


Fig.14. uniformization CD comparison between break troughsteps temperature 60cand 20c. The temperature of othersteps is 60c.

We are both conscious that corrosion often occurs on sidewalls with patterned surfaces after a dry metal plasma etch with residue (chlorine species). The four sides of the D-film, which is why metal D was absent from the problem seen in fig.14(a), would produce a post etch stain in our RRAM model. An even more serious corrosion.

Metal C etching was performed with plasma based on Cl2/BCl3. Two steps have been taken to discourage corrosion: 1. Enhance the BCl3/Cl2 gas ratio; 2. Using N2 and CH4 sidewall gasses. The suitable TE profile shown in Fig.6 can be obtained by a proper optimization etch with those two acts.

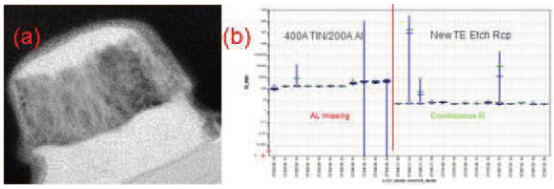


Fig. 16. (a) TEM image of TE etch which shows metal D exists.

(b) TE Rs comparison between metal D missing and exists condition.

The final yet most critical problem in metal b trench etch seen in Fig. 14(b) is a concern with TE / metal B relationships. Because of the different etching rates between BD in the logical region and HM oxide in the RRAM cell area, the remaining HM post-metal B etch doesn't bind TE to metal B. In other terms, if the trench depth of the thinking area exceeds the goal, HM will continue.

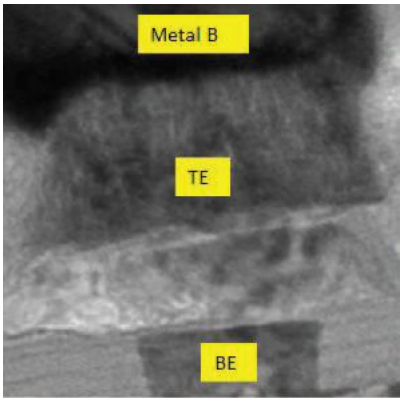


Fig.17. TEM image of RRAM cell post metal B trench etch..

Tin A by elimination of liner is used in the tin B grain grain recette that is opened with NDC liner, and the remainder of the HM is used for solution collection between NDC and HM oxides. Metal A can be obtained by elimination of the cover. As a result, HM is removed by removing oxide liner into NDC. In addition, the question of TiN oxidation has been seen in. The NDC HM wafer post-metal B trench etch yield should be prevented as seen in Fig.17. The strong relation between TE and metal B is clear.

By observing the survey carried out we can conclude that the current memory devices can observe more transistor, power hence the memristor based memory can be implemented as shown in the below section.

V. RESULT AND EXPERIMENTAL DISCUSSION

The memristor is as shown in the below figure, which has employed the AND and OR logic to implement the full adder. By using the memristors to implementation the number of transistors, power consumed are lesser compared to existing full adder using MOSFET.

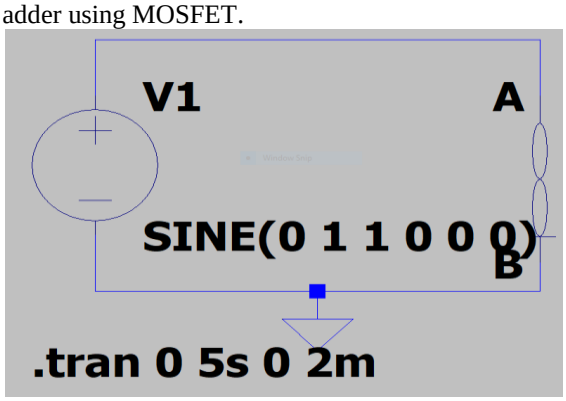


Fig. 18 Memristor Circuit

The results of the two memristor are showed in the below figure,

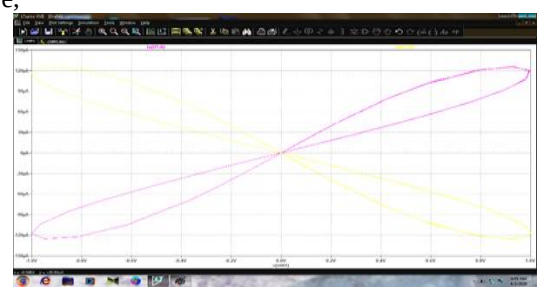


Fig 19. First Memristor result.

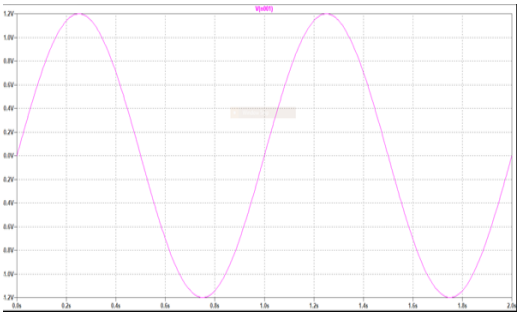


Fig 20. Second memristor result

The below figure shows the implementation of AND gate using memristor.

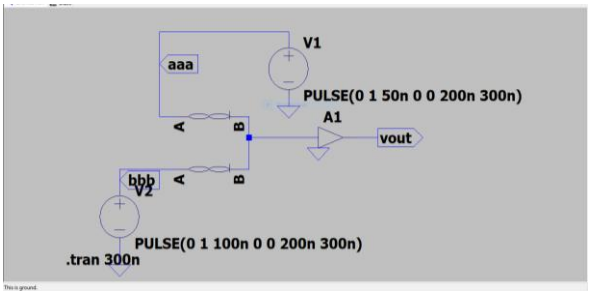


Fig 21. Implemented block of AND gate using Memristor.

The result of the implemented AND gate block is shown in the below figure, the waveform shows that the results obtained are right.

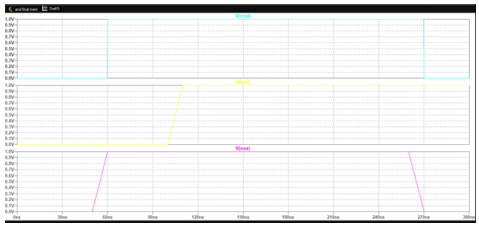


Fig 22: AND gate Results for Memristor.

The below figure shows the implementation of OR gate using memristor.

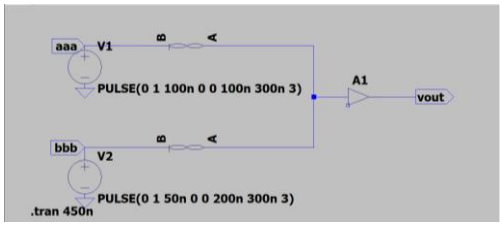


Fig 23: OR gate results for Memristor.

The result of the implemented OR gate block is shown in the below figure, the waveform shows that the results obtained are right

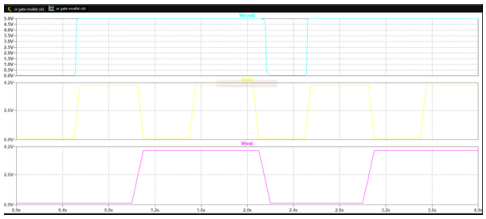


Fig 24: OR gate Results for Memristor.

The memristor are used to implement the full adder and it is as shown in the figure 25.

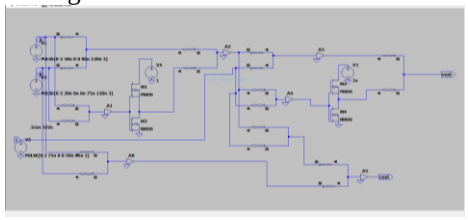


Fig 25: Full adder implementation using Memristor.

The below figure shows the implementation of Full adder using memristor

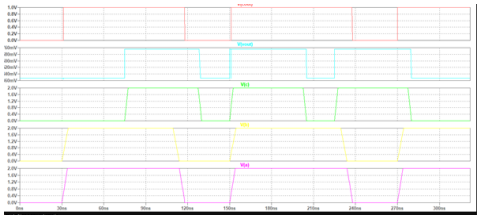


Fig 26: Full adder waveforms using Memristor.

VI. CONCLUSION

This paper analyzed the latest developments in the production of memory. Because of their smaller size and low power consumption, most circuits rely on the VLSI architecture. This paper analyzed the 58 papers concerned with the creation of the memory cup to substitute the original memory cup. The full adder is implemented using the Memristor AND/OR logic with lesser transistors as shown in figure 18. The results are found satisfactory with respect power consumption, number of transistors.

Throughout addition to this, the power usage, the region and pace correlated with the configuration of the memorizers are all listed. Finally, the work void for the papers is generated by the review.

REFERENCE

1 I. G. Baek, D. C. Kim, M. John Lee, et al., "OxRRAM, for a Post-storage use, multi- cross- binary oxide resistive memory" in IEEE Int. IEDM Inc. IEDM Inc. Dig., Dec. 2005, 750–753. Dig.

2 K. Huang, J. M. Tseng, C. W. Hsu, et al., IEEE ElectronDevice Lett., vol.: Bipolar nonlinear Ni / TiO2/NI choice for 1S1R crossbar array applications. 32, p. 10, 1427-, Oct. 2011. Oct.

3 R. Waser and M. Waser. Aono, "Memories of resistive transition dependent on nanoionics," Natural Mater., vol. 6, no. 11, pp. 833-, November 2007.

4 S. K .- H. Kim, H. Jo, and W. Lu, "Programmable two- nanoscale resistance flipping," Nano Lett., vol. 9, no. 1, 496–500, Dec. 2008. 2008.

5 H. Y. Lee et al.:"Low power and high- bipolar switching in flexible HfO2-based RRAM with a thin reactive Ti buffer layer, "in IEDMTech. Dig., Dec. 2008, pages 1–4.

6 H. Lv, H. Wan, T. Tang, "Introducing thin GST interfaced layer to improve resistive switching uniformity," IEEE ElectronDevice Lett., vol. 31, no. 9, pp. 978-, September 2010.

7 S. Long et al., 'Voltage and power regulated HFO2-based RRAM transfer schemes,' Sci. Sci. Long et al. Rep., f. Rep. 3, No. 3, Oct. 2013, p. 2929.

8 Chen, C.H. Tsai Y.S. Chen, P.S., P.Y. Gu, H.Y. Lee, , T.Y. Wu, K.H. Tsai, S.S. Sheu, W.P. Lin, C.H. Lin, P.F. Chiu, W.S. Chen, F.T. Chen, C. Lien, and M.-J. Tsai, "Challenges and Opportunities for HfOX Based Resistive Random Access Memory", *IEDM Tech. Dig.*, 2011, pp717-720.

9 L. Zhang, B. Govoreanu, A. Redolfi, D. Crotti, H. Hody, V. Paraschiv, S. Cosemans, C. Adelmann, T. Witters, S. Clima, Y.-Y. Chen, P. Hendrickx, D. J. Wouters, G. Groeseneken, and M. Jurczak, "High-drive current (>1 MA/cm2) and highly nonlinear (>103) TiN/amorphous-silicon/TiN scalable bidirectional selector with excellent reliability and its variability impact on the 1S1R array performance," in *IEDM Tech. Dig.*, Dec. 2014, pp. 6.8.1–6.8.4, doi: 10.1109/IEDM.2014.7047000.

10 L. Zhang, A. Redolfi, S. Adelmann, C. Clima, I. P. Radu, D.J. Chen, D. J. Wouters, M. Jurczak and G. Groeseneken. Govoreanu, "Bipolar RRAM selector applications ultrathine, silicone / amorphous diode," IEEE Electron System Lett., vol. 31, No. 2, 199–2014, February 2014, Di: 10,1109/LED.2013.2293591.

11 J. Yang *et al.*, "Memristive devices for computing,"*Nature Nanotechnology, Vol. 8*, pp. 13 – 24, Jan. 2013.

12 Z.Jiang *et al.*, "Verilog-A compact model for oxide-based resistive random access memory (RRAM)," in *Proc. of Int. Conference on Simulationof Semiconductor Processes and Devices (SISPAD)*, Sept. 2014, pp. 41 – 44.

13 P.-Y. Chen and S. Yu, "Compact modeling of RRAM devices and its applications in 1T1R and 1S1R array design," *IEEE Transaction on Electron Devices, Vol.62, No. 12,*, pp. 4022 – 4028, Dec. 2015.

14 J. Strachan *et al.*, "State dynamics and modeling of tantalum oxide memristors," *IEEE Transactions on*

15 *Electron Devices, Vol. 60, No. 7,*, pp. 2194 – 2202, Jul.2013.

16 W. Wang *et al.*, "Nonvolatile SRAM cell," in *Int.Electron Devices Meeting (IEDM)*, Dec. 2006, pp. 27 –30.

17 S.Yamamoto *et al.*, "NonvolatileSRAM (NV-SRAM) using functional MOSFET merged with resistive switching devices," in *IEEE Custom IntegratedCircuits Conf. (CICC) Tech. Dig. Papers*, Sep. 2009, pp. 531 – 534.
18 P.-F. Chiu *et al.*, "Low Store Energy, Low VDDmin, 8T2R Nonvolatile Latch and SRAM With Vertical-Stacked Resistive Memory (Memristor) Devices for Low Power Mobile Applications," *IEEEJournal of Solid-State Circuits, Vol. 47, No. 6,*, pp. 1483 – 1496, Jun. 2012.
19 M.-F. Chang *et al.*, "Endurance-aware circuit designs of nonvolatile logic and nonvolatile SRAM using resistive memory (memristor) device," in *Proc. Asiaand South Pacific Design Automation Conference(ASP-DAC)*, Feb. 2012, pp. 329 – 334.
20 V. Betz, J. Rose, A. Marquardt, Deep-Submicron FPGAS Architecture and CAD. Boston, MA, United States: Kluwer, 1999.
21 R. [23] R. R. Dittmann and R. Muenstermann, T. Menke. Waser, "Coexistence of thin-film thin-film memristive devices for filamentary and homogenous resistive transition," Adv. Mater. Vol. Mater. 22, no. 43, p. 4819–4822, 2010. 2010.
22 H. Okushi, M. Saito, M. Kikuchi and Y. Hirai, "Polarized (letter '8') hetero- and non-hetero-system memory effects," Solid State Society, vol. 11, No. 1, 283–286, 1972. 1972.
23 M .- J. "The 2-stack 1D-1R cross-point oxide diode structure, as switch elements for RAM applications with high density resistance," Lee, et al. in Proc. Int. IEEE. Meeting on Electron Systems, Dec. 2007, pp. 771-774.
24 Sasago et al., in Proc.: "Cross-point memory transition with 4F2 cell size powered by low-contact poly-si resistivity diode." Symp. VLSI IEEE technology. (VLSIT), June 2009, pages 24-25.
25 G. Tallarida et al., "Non-volatile memory crossbar temperature rectifier junctions," in Proc. Int. IEEE. Workshop Memories, May 2009, pp. 1–3.
26 K. K. Gopalakrishnan et al., "Mixed ionic electronic conduction material (MIEC) ultra-scalable novel access system for high density phase memory shift (PCM) arrays," Proc. Symp IEEE. VLSITechnology. (VLSIT), June 2010, pages 205-206.
27 Y. Liauw, Z. Zhang, W. Kim, W. Kim, A. E. Gamal, S. S. Wong, "Non-volatile RRAM-configuration memory 3D-FPGA stacked monolithically," in Proc. Int. IEEE. Conf.,Feb, Solid-State Circuits. 2012, pages 406–408.
28 Y .- C. [32] W. Wang, Chen, W. Li and W. Zhang, "Non-volatile RRAM-based 3D stacking FPGA," in Proc. Twenty-second Int. Conf. Conf. Land Program. Computer Program. LogicAppl., 2012, pp. 41-76.
29 W. W. Wang, T. T. Jing, B. Butcher, "FPGA focused on memristor and CMOS integration," in Proc. Int. IEEE. Good. Good. SystemCircuits. SystemCircuits. (ISCAS), June / May. 2010, p. 1963–66. 2010.
30 F. C. C. E. and Hoppensteadt. M. Izhikevich, IEEE Trans. Neural Network, vol., "Pattern Detection in Step Based Neural Loop Networks." 11, No. 3, May 2000, pp. 734–738.
31 Hoppensteadt. M. Izhikevich, 'Laser oscillator synchronization, associative memory and neurocomputing optics,' Phys. Rev. F, f. B, e. 62, no. 3, 4010–4013, 2000. 2000.
32 Hoppensteadt. Izhikevich, "Mechanical resonator synchronization and neurocomputing," IEEE Trans. SystemCircuits. I, Company. I, Program. Appl. Philosophy, vol. 48, p. 2, 133–138, February 2001.
33 R. Wooden and K. Krischer, "Easy oscillatory circuit pattern detection," New J. Phys., vol. 13, p. 7, 073031, 2011.
34 S. Kaka et al., "Mutual step locking of nanooscillator microwave spin torque," Nature, Vol. 437, vol. 7057, 389–392, 2005.
35 R. Waser, M. Aono, "Resistive Switching Memories dependent on nanoionics," Nature Mater, vol. 6, 11, pp. 833-840, 2007.
36 D.Ielmini, "Field and temperature-driven filament development, model universal set / reset characteristics for bipolar RRAM," IEEE Trans. Electron Devices, vol. 58, no. 12, 4309-4317, Sep. Dec.
37 D.-H. Kwon *et al.*, "Atomic structure of conducting nanofilaments in TiO resistive switching memory," *Nature Nanotechnol.*, vol. 5, no. 2, pp. 148–153, 2010.
38 M. Noman *et al.*, "Mechanism of localized electrical conduction at the onset of electroforming in TiO2 based resistive switching devices," *Appl. Phys. Lett.*, vol. 104, no. 11, p. 113510, 2014.
39 S. Yu and H.-S. Wong, "A phenomenological model for the reset mechanism of metal oxide RRAM," *IEEE Electron Device Lett.*, vol. 31, no. 12, pp. 1455–1457, Dec. 2010.
40 B. Gao *et al.*, "Unified physical model of bipolar oxide based resistive switching memory," *IEEE Electron Device Lett.*, vol. 30, no. 12, pp. 1326–1328, Dec. 2009.
41 J. Kwon, A. A. Sharma, J. A. Bain, Y. N. Picard, and M. Skowronski, "Oxygen vacancy creation, drift, and aggregation in TiO2-based resistive switches at low temperature and voltage," *Adv. Functional Mater.*, 2015.
42 Z. Wang *et al.*, "Highly uniform, self-compliance, and forming-free ALD-based RRAM with GE doping," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 1203–1208, Apr. 2012.
43 L. Zhao *et al.*, "Multi-level control of conductive nano filament evolution in HfO ReRAM by pulse-train operations," *Nanoscale*, vol. 6, no. 11, pp. 5698–5702, 2014.
44 I. Baek, D. Kim, M. Lee, et.al "Multi-layer cross-pointbinary oxide resistive memory (OxRRAM) forpost-NAND storage application," in IEDM Tech. Dig.,2005, pp. 750–753.
45 Y. Hosoi, Y. Tamai, T. Ohnishi, K. Ishihara, et, al, "High speedunipolar switching resistance RAM (RRAM) technology," in*IEDM Tech. Dig.*,2006, pp. 793–79.
46 S. Seo, M. J. Lee, D. H. Seo, et.al, "Reproducible resistanceswitching in polycrystalline NiO films," *Appl. Phys. Lett.*, vol.85, p. 5655, 2004.
47 B. Govoreanu et al, "10x10nm2 Hf/HfOx Crossbar ResistiveRAM with Excellent Performance, Reliability and Low-EnergyOperation," *IEDM Tech. Dig*, p.729, 2011.
48 H.-S. P. Wong, H.-Y. Lee, S. Yu, Y.-S. Chen, Y. Wu, P.-S. Chen,B. Lee, F. T. Chen, and M.-J. Tsai, "Metal–Oxide RRAM,"Proc. IEEE, vol. 100, no. 6, pp. 1951–1970, 2012.
49 YU Chen and Shimeng Yu ,"compact modeling of RRAM deices and its Aplication in 1T1R and 1S1R Array design.IEEE transaction on electron devices,vol 62,no 12, December 2015.
50 Bang, S.; Kim, M.; Kim, T.; Lee, D.; Kim, S.; Cho, S. Gradual switching and self-rectifying characteristics ofCu/_-IGZO/p+-Si RRAM for synaptic device application. Solid State Electron. **2018**, 150, 60–65.
51 Bertolazzi, S.; Bondavalli, P.; Roche, S.; San, T.; Choi, S. Nonvolatile Memories Based on Graphene and Related 2D Materials. Adv. Mater. **2019**, 31, e1806663.
52 Bukke, R.N.; Avis, C.; Jang, J. Solution-Processed Amorphous In–Zn–Sn Oxide Thin-FilmTransistor PerformanceImprovement by Solution-Processed Y2O3Passivation. IEEE Electron Devices Lett. **2016**, 37, 433–436.
53 Tian, M.; Zhong, H. E_ects of Electrode on the Performance of Al2O3 Based Metal-Insulator-Metal Antifuse.ECS J. Solid State Sci. Technol. **2019**, 8, N32–N35.
54 Rodriguez-Fernandez, A.; Aldana, S.; Campabadalm, F.; Sune, J. Resistive Switching with Self-Rectifying Tunability and Influence of the Oxide Layer Thickness in Ni/HfO2/n+-Si RRAM Devices. IEEE Trans.Electron Dev. **2017**, 64, 3159–3166.
55 Wu, X.; Cha, D.; Bosman, M.; Raghavan, N.; Migas, D.; Borisenko, V.; Zhang, X.; Li, K.; Pey, K.Intrinsic nanofilamentation in resistive switching. J. Appl. Phys. **2013**, 113.
56 Lee, J.; Schell, W.; Zhu, X.; Lu, W. Charge Transition of Oxygen Vacancies during Resistive Switching inOxide-Based RRAM. ACS. Appl. Mater. Interfaces **2019**, 11, 11579–11586.
57 Sarkar, B.; Lee, B.; Misra, V. Understanding the gradual reset in Pt/Al2O3/Ni RRAM for synaptic applications.Semicond. Sci. Technol. **2015**, 30.
58 Wu, L.; Dong, C.; Wang, X.; Li, J.; Li, M. Annealing e_ect on the bipolar resistive switching memory of NiZnferrite films. J. Alloys Compd. **2019**, 779, 794–799.
59 Ram, J.; Kumar, R. Effect of Annealing on the Surface Morphology, Optical and and Structural Properties ofNanodimensional Tungsten Oxide Prepared by Coprecipitation Technique. J. Electron. Mater. **2018**, 48, 1174–1183.

AUTHORS PROFILE

Ravikumar K. Is a research scholar pursuing a Ph.D. from Jain University, JGI Global Campus, Bengaluru, Karnataka, India. He has secured distinction with the Third rank in Visvesvaraya Engineering Technology, Belgavi, Karnataka, M.Tech VLSI Architecture and Embedded Systems 2012. In 2010 he ended his studies in Instrumentation Engineering from Visvesvaraya Technological University, Belgavi, Karnataka.

Dr. Sukumar R has completed his B.E. 1992 ECE from University of Madurai Kamaraj, M.E. In 2004, at CSE, ManonmaniumSundaranar University and in 2010 at Anna University. Ph.D. He has over 205 years of experience teaching from a beginner to a doctoral degree. He is also a well proven PhD Instructor at Anna Chennai University and Jain Bangalore University. Four graduates have now earned Ph. D under his guidance and seven graduate students. He is also a member of the Studies Committee and numerous commissions. This includes more than 30 international journal publications and 20 foreign conference publications. He is presently Professor and Head of ECE at Jain University College of Engineering & Technology, JGI Global Campus, Bangalore, India. He has focused on cryptography & network encryption, sensor networks, cloud and IoT.