International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9, Issue-7, May 2020

A New Asymmetrical MLI with Reduced Switch Count for a Three Phase Induction Motor

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Abstract: ***This work explores a novel multilevel inverter (MLI) topology to minimize the number of power switches in the passage of current to accomplish each level of the output voltage. The unequal magnitudes of the dc voltage sources in attempt to realize higher levels of the output voltage bring in the asymmetrical nature of operation. It involves a series parallel switched configuration with bidirectional switches to avert the flow of circulating current in between the two H - bridges in each phase of the MLI. The effort incites to use the theory of a new Pulse Width Modulation (PWM) strategy for mitigating the higher frequency components of the voltage applied to the stator. It imbibes the Phase Disposition (PD) principles in the modulating strategy for arriving at the sinusoidal shape for the output voltage . Total Harmonic Distortion (THD) indexed by lower values for the output voltage over the traditional firing scheme serves to be the highlight for the MLI in acclaiming its place in the inverter world. The results obtained through MATLAB based simulation over a range of modulation indices. The performance measured in terms of the THD claims its suitability for use in Induction Motor (IM) drives.***

Keywords : Induction motor, Total harmonic distortion , Phase disposition , Pulse width modulation, Series parallel switched multilevel inverter.

I. INTRODUCTION

The IM drives form part of the industrial encomiums and play an exquisite role in enabling variable speed control applications for industrial outfits. The medium voltage motor drives experience difficulty to connect only one power semiconductor switch directly to the grid [1] . Besides the requirements envisage changing the operating characteristics of the power apparatus for reaching out to specific attributes. In light of their capability to operate at high voltages, the MLIs continue to call attention and offer a higher efficiency. The rise in the number of output stages forges to minimize the output voltage distortion and use lower blocking voltage switches [2]. It allows higher output voltages to be produced, while at the same time raising the stress on the semiconductor device. The desired output voltage waveform synthesized from the multiple voltage levels fosters as an efficient solution to increase the power output and reduce the harmonic content of the ac waveform.

Revised Manuscript Received on May 30, 2020.
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The advantages include both static and dynamic voltage sharing between the active switches. In high-power motor drives used in traction drives shipyard, petrochemical industries and transmission of high-power the MLIs find extensive role. It augurs a gap in distributed energy systems where input side batteries, fuel cells, solar panels, and rectified wind turbines form the dc source[3]. The ac output voltage received from the inverters enters direct support of a load or interconnects to the ac grid without problems with the voltage balancing. A new MLI topology was introduced, and subsequent modules were obtained from a sequence of essential block connections. It was analyzed using both symmetric and asymmetric operating modes, and the presentation of comparative analysis with conventional topology[4]. For checking the outcomes of the computer simulation a prototype was implemented. A new MLI architecture was developed and generalized using the fundamental block series relation. It was tested in both modes of symmetric and asymmetric operation and deliver various voltage rates with minimal semiconductor switches[5]. To check the effects of the computer simulation, a laboratory prototype was built. For a thirteen level asymmetric inverter, a new PWM approach which offers less dv / dt and lower THD to the voltage waveform was suggested [6]. It was presented to confirm unidirectional flow of power in every inverter cell and the simulation and hardware outputs were given. In spite of the circumstance that numerous topologies emerge, still modifications require to provide scope for expanding the use of MLI.

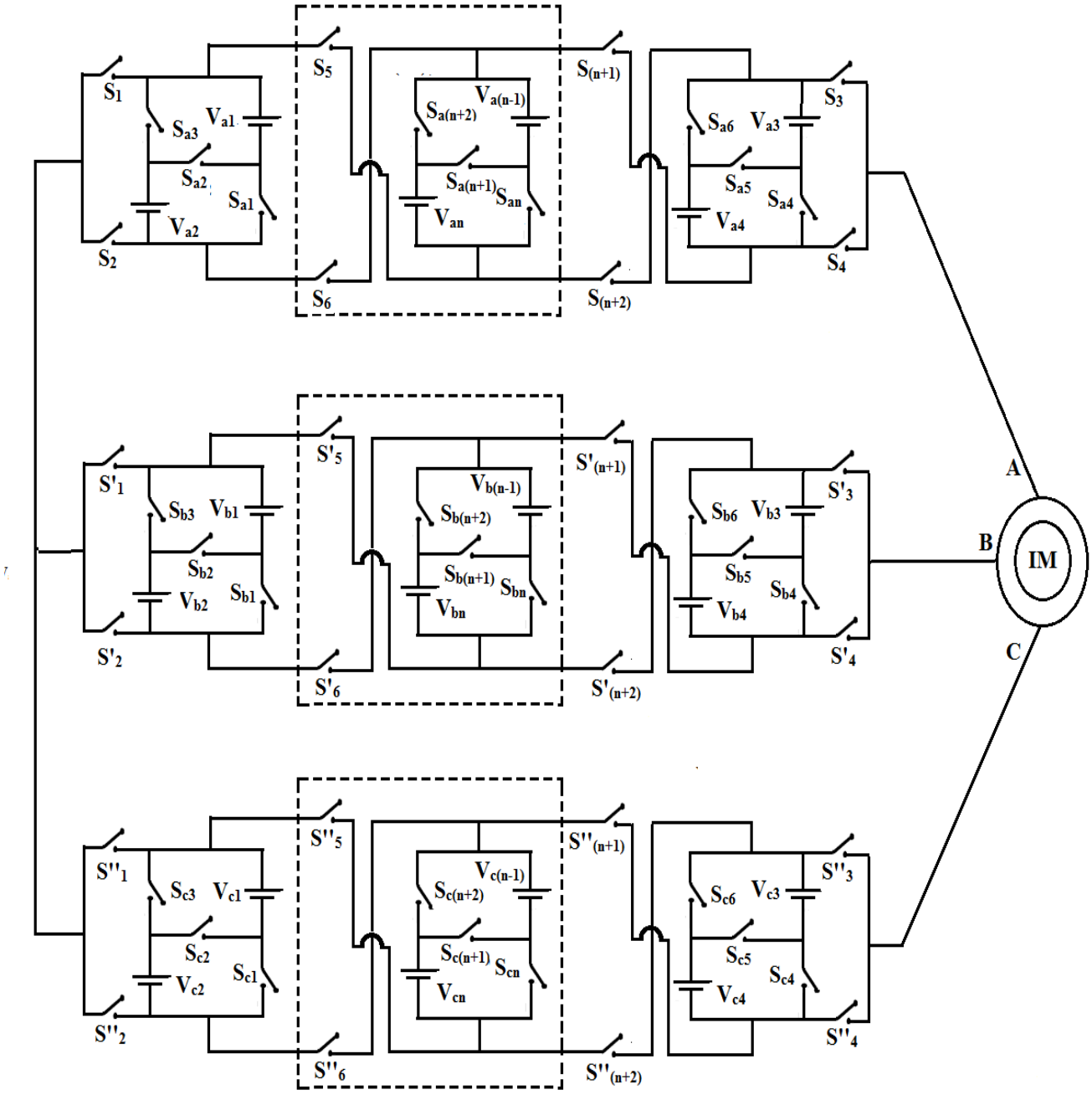
II. PROBLEM STATEMENT

The main emphasis owes to derive an asymmetrical configuration for the proposed series parallel switched multilevel inverter (SPSWMLI) and ensuring that it requires the use of a least number of switches to achieve each level of the output voltage. The design attempts to observe the choice of different modulation principles in generating the PWM pulses for arriving at the least value for the THD of the stator voltage. The research discusses the MLI's output by simulation, and shows the realistic suitability of its use.

III. PROPOSED METHODOLOGY

The focus centers on configuring the SPSWMLI to offer different levels of variable output voltage for the three phase IM. It entices to minimize the switches used in the path for the flow of current in each mode of operation. The methodology echoes the usage of a new PWM strategy in an attempt to minimize the output line and phase voltage THD. The generalized structure of the SPSWMLI shown in Fig. 1 comprises of two similar cells,

each constructed with a switch together with a dc source in both the arms and a switch between the arms of the cell. It brings in H-bridges along the sides of the both the cells, adds two bidirectional switches to interconnect the two portions and connects the IM across. them. It allows extending the structure on either side to pave way for raising the number of stages in the output voltage



The operating switches in Fig.2 trace the path of the current in the MLI to obtain the A phase voltage.

IV. MODES OF OPERATION

The unidirectional switches (S_1 - S_4), (S_1' - S_4'), (S_1" - S_4") forms the H-bridge inverters respectively in the three phases with S_{a1}…. $S_{a(n+2)}$, S_{b1}…. $S_{b(n+2)}$ and S_{c1}…. $S_{c(n+2)}$ enabling the path for the current to flow. The bidirectional switches S_5 S_6, S_5', S_6', S_5", S_6" in the link that connects the two H-bridges serve to prevent the flow of circulating current within the H-bridges in each cell.

The Figs. 3 to 6 relate to the operating modes of the MLI to produce $+5V_{DC}$ and $-5V_{DC}$ and $+8V_{DC}$ and $-8V_{DC}$ as part of the seventeen level output for the A phase and the data`s in Table 1 show the corresponding switches for every mode for the A phase. It engraves the same sequence for the use of the switches to account for the output of the other two phases.

The power switches required to obtain increasing levels of output voltage per phase for both the new SPSWMLI and the Cascaded H-Bridge Multilevel Inverter (CHBMLI) follows the relation (5k+2) and (8k) respectively and k stands for the number of cells .

From the relation it shows that the reduction in the switch count for the new SPSWMLI over the CHBMLI for the equal number of dc sources.

Table 1 Conduction Sequence of seventeen level operation for A Phase

Levels of Output Voltage	Switches Conduction											
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_1	S_2	S_3	S_4	S_5	S_6
$+V_{DC}$	√		√					√		√	√	
$+2V_{DC}$		√						√		√	√	
$+3V_{DC}$				√		√	√		√		√	
$+4V_{DC}$	√		√	√		√		√	√		√	
$+5V_{DC}$		√		√		√		√	√		√	
$+6V_{DC}$					√		√		√		√	
$+7V_{DC}$	√		√		√			√	√		√	
$+8V_{DC}$		√			√			√	√		√	
$0V_{DC}$							√		√		√	
$-V_{DC}$	√		√				√		√			√
$-2V_{DC}$		√					√		√			√
$-3V_{DC}$				√		√		√		√		√
$-4V_{DC}$	√		√	√		√	√			√		√
$-5V_{DC}$		√		√		√	√			√		√
$-6V_{DC}$					√			√		√		√
$-7V_{DC}$	√		√		√		√			√		√
$-8V_{DC}$		√			√		√			√		√

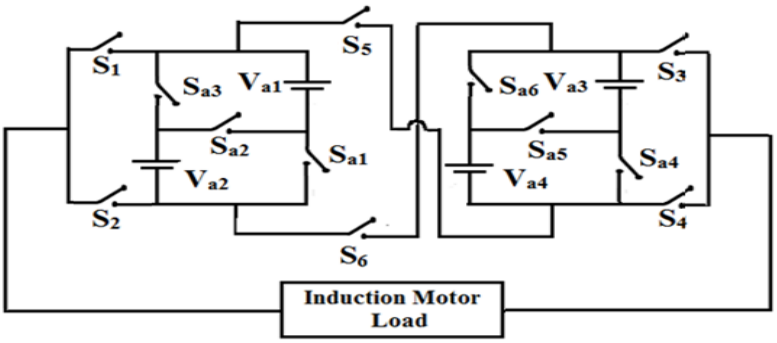


Fig. 2 SPSWMLI for seventeen-level output for A Phase

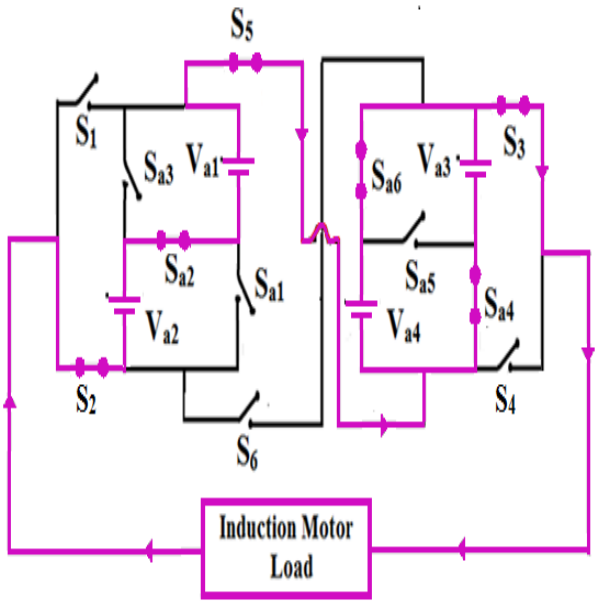


Fig. 3 Operating modes for +5V_{DC}

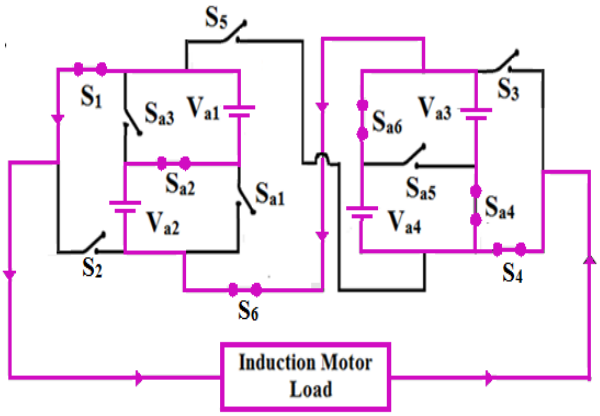


Fig. 4 Operating modes for -5V_{DC}

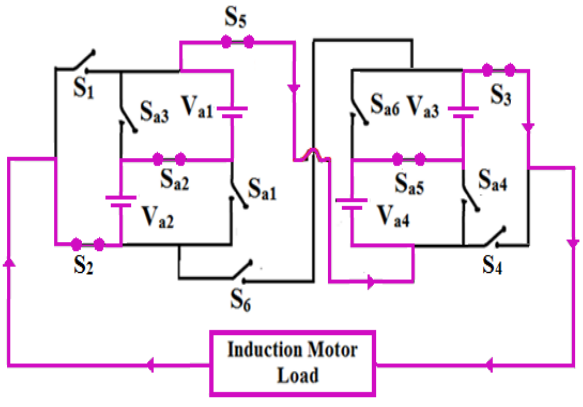


Fig. 5 Operating modes for +8V_{DC}

V. MODULATION STRATEGY

The philosophy of PWM exerts a mechanism to control the output voltage of the inverter. It accomplishes the facility through an adjustment in the ON and OFF periods of the power switch in each operating mode. The terms of duty cycle and frequency characterize the features of any PWM signal and manifest its influence in the successful compliance of the inverter output.

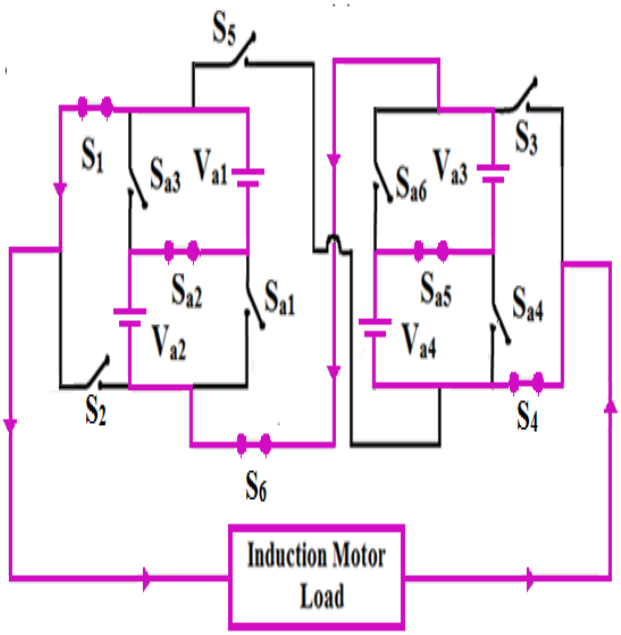


Fig. 6 Operating modes for -8V_{DC}

While the duty cycle measures the period of time the signal remains in the on state, the frequency estimates the speed at which the PWM completes a cycle. The multilevel sinusoidal pulse width modulation (SPWM) allows the sinusoidal reference signal to be compared with a variety of options for the carriers to produce the PWM signal.

The methodology relates to a new strategy for extracting pulses from the initial and final 60^o interval of each half cycle of a full sinusoidal wave in order that it experiences a change only across this portion of the reference signal and as a consequence allows a change in the modulation index [7]. The advantages follow to offer rise in the fundamental component of both the stator phase and line voltage of the IM and a decrease in their THD.

The principle includes the usage of PWM activity based on carrier disposition to produce the switching pulses in the MLI for the power devices. It owes the option between the PD that enables carriers to align in phase, alternative phase opposition disposition that generates a 180^o phase change between carriers and carrier polarity variation where the carriers' polarity remains in a band.

The PD-based method gives more preference since it contrasts the carrier signals of the similar frequency, amplitude and phase with a dc offset, which occupies various levels in a single sine modulating signal and helps to offer high load voltage with lesser THD.

The combinatorial functions in Fig .7 augur the logical synthesis of operations for arriving at the intersecting points of the triangular carrier waves and the sinusoidal reference to derive the PWM pulses for the switches. The Table 2 contains the comprehensive summary of the types of logical operators required to pull out the pulses for the switches in A phase .

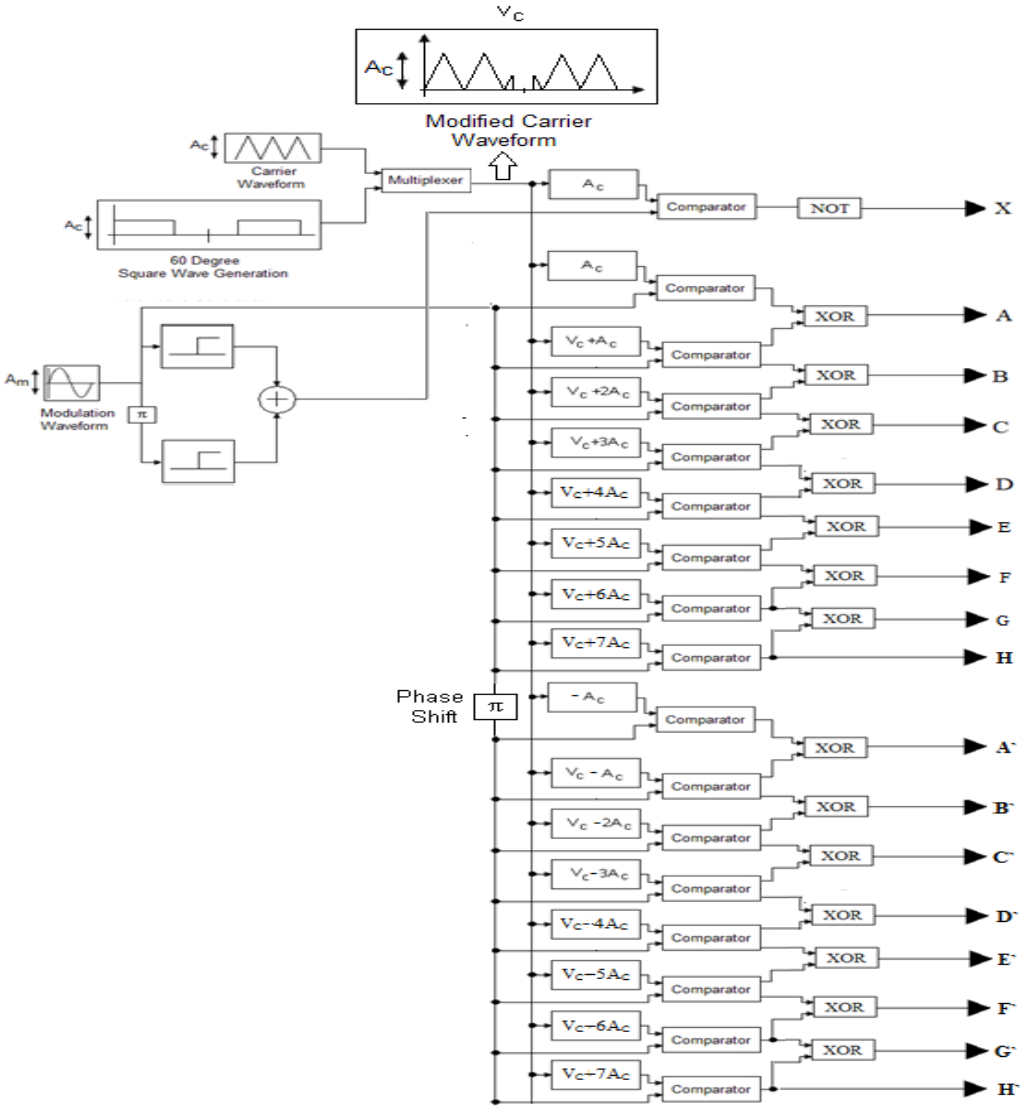


Fig. 7 Production of PD Multicarrier - 60^o PWM pulses for A Phase

VI. SIMULATION RESULTS

The procedure orients to obtain a variable sinusoidal voltage for operating a 415Volts, 1HP, 1410RPM, three phase squirrel cage IM through the new asymmetrical MLI interface. It forges to examine the performance of the new multicarrier PWM scheme on the three phase MLI driven from 40 Volts dc source (V_{a1}=V_{a2}= V_{DC} = 40V) in the first H-bridge and 120 Volts dc (V_{a3}=V_{a4}= 3V_{DC} = 120V) in the second on a MATLAB/SIMULINK platform.

The produced PWM pulses exposed in Figs.8 to 10 agree the devices to be switched via the PD-based Multicarrier-60^o PWM in each step of its operation. The output phase and line voltage waveforms seen in Figs.11 to 14 found from the PD-based Multicarrier-60^o PWM and the multicarrier pulse width modulation (MCPWM) corresponds to 0.5 Kw operating load. The structure of the waveforms shows the fitness of the proposed PWM for achieving an almost sinusoidal pattern.

Figs.15 to 18 compare the phase and line output voltage THD spectra obtained with a modulation index of 1 and 0.5Kw operating load for PD based multicarrier 60^o PWM and the MCPWM. The efficiency of the output phase voltage projected using the bar diagram in Fig.19 enumerates the efficacy of the proposed modulation scheme over MCPWM. The phase voltage variation with THD shown in Fig.20 for a variety of modulation indices for the different PWM methods shows the advantages of the new modulation scheme produce higher RMS magnitudes values.

The same findings for line voltage in Table. 4 further add power to elucidate the Multicarrier 60^o PWM strategy. The speed, torque and steady state current waveforms in Fig. 21 relate to the same operating point for the IM. It exhibits the capability of the motor to adapt the sudden increase of 0.5Kw load subjected at 1 second and operate at the new operating point

Table 2 Switching table for generation of PD Multicarrier - 60^o PWM pulses for Phase A

Switches	Logical functions
S_{a1}	A (OR) D (OR) G (OR) A' (OR) D' (OR) G'
S_{a2}	B (OR) E (OR) H (OR) B' (OR) E' (OR) H'
S_{a3}	A (OR) D (OR) G (OR) A' (OR) D' (OR) G'
S_{a4}	C (OR) D (OR) E (OR) C' (OR) D' (OR) E'
S_{a5}	F (OR) G (OR) H (OR) F' (OR) G' (OR) H'
S_{a6}	C (OR) D (OR) E (OR) C' (OR) D' (OR) E'
S_1	A (OR) B (OR) D (OR) E (OR) G (OR) H (OR) C' (OR) F'
S_2	C (OR) F (OR) A' (OR) B' (OR) D' (OR) E' (OR) G' (OR) H'
S_3	A (OR) B (OR) C' (OR) D' (OR) E' (OR) F' (OR) G' (OR) H'
S_4	C (OR) D (OR) E (OR) F (OR) G (OR) X (OR) A' (OR) B'
S_5	X (OR) A' (OR) B' (OR) C' (OR) D' (OR) E' (OR) F' (OR) G' (OR) H'
S_6	A (OR) B (OR) C (OR) D (OR) E (OR) F (OR) G (OR) H

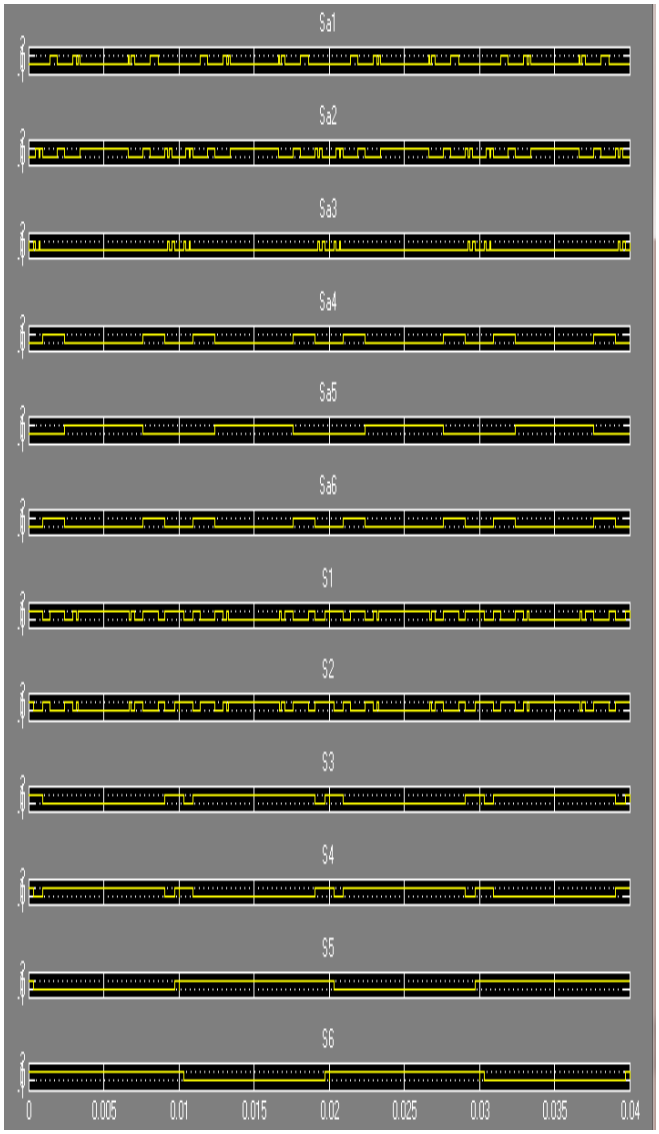


Fig. 8 Gating pulses for A Phase

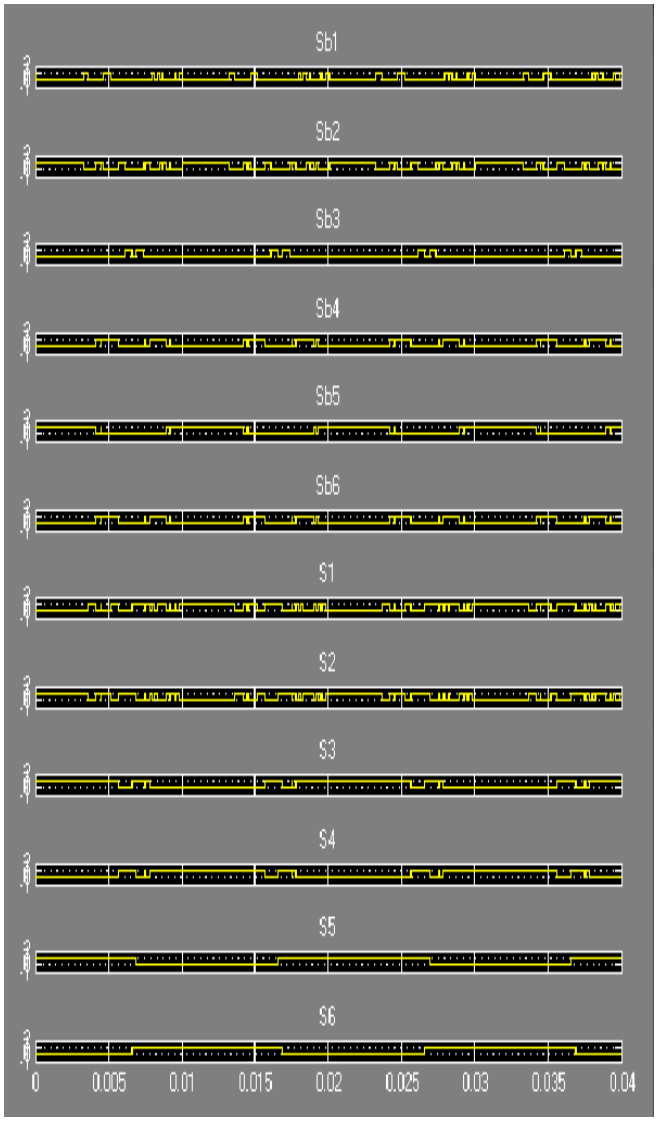


Fig. 9 Gating pulses for B Phase

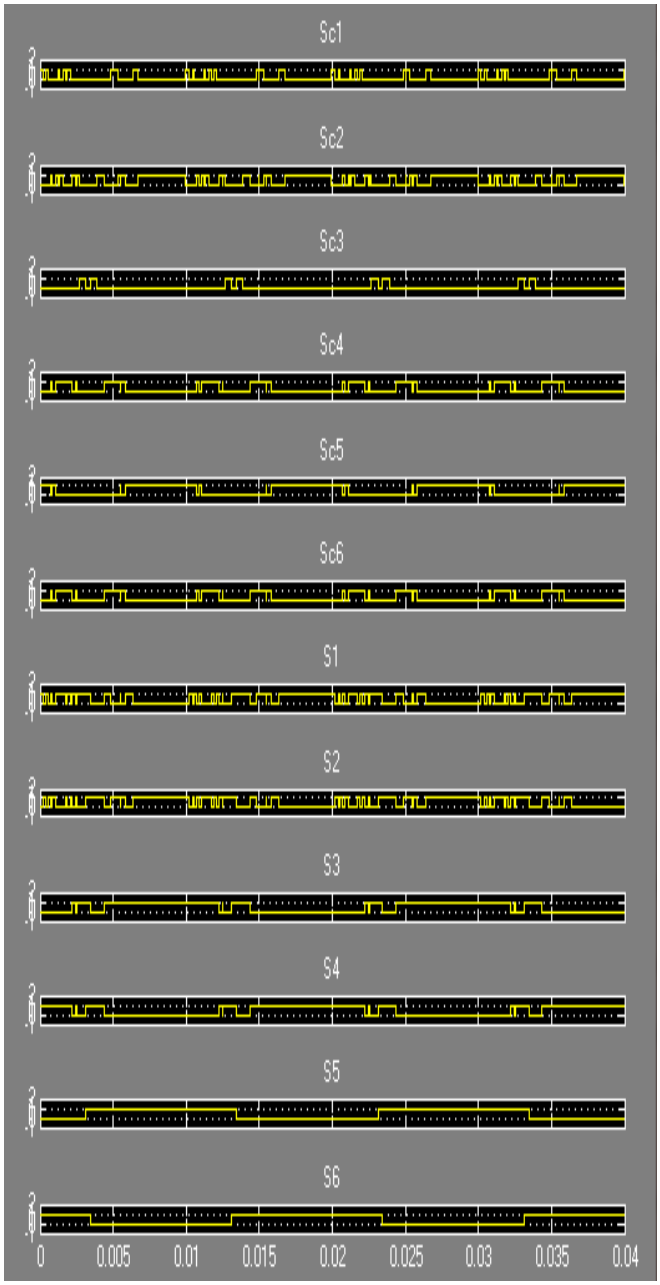


Fig. 10 Gating pulses for C Phase

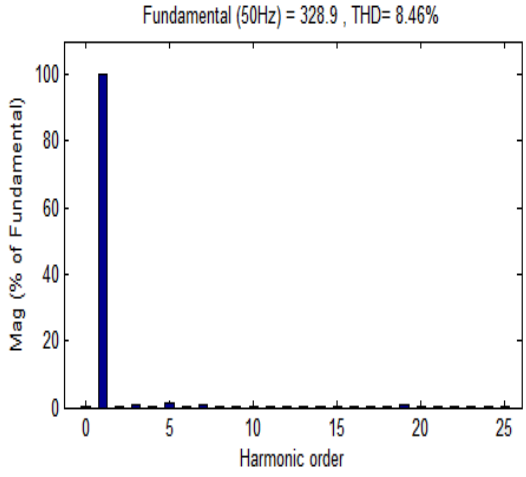


Fig. 11 Phase voltage (V_a) THD for PD MCPWM

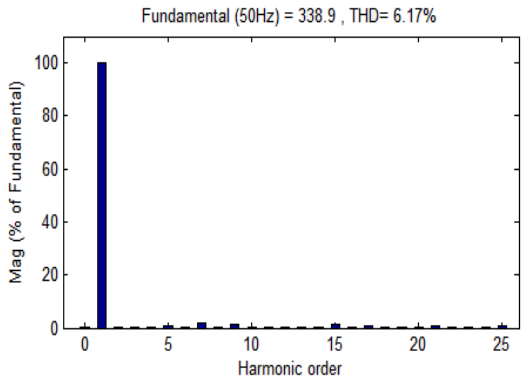


Fig. 12 Phase voltage (V_a) THD for PD Multicarrier - 60° PWM

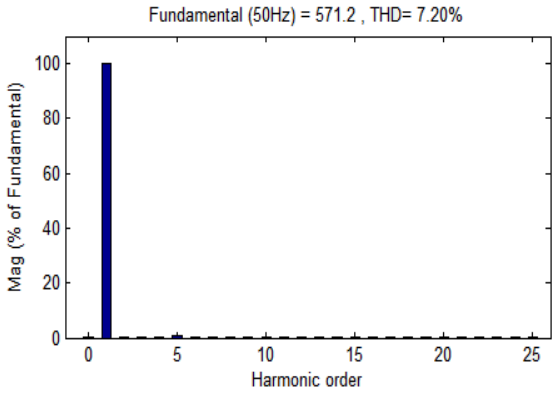


Fig. 13 Line voltage (V_{ab}) THD for PD MCPWM

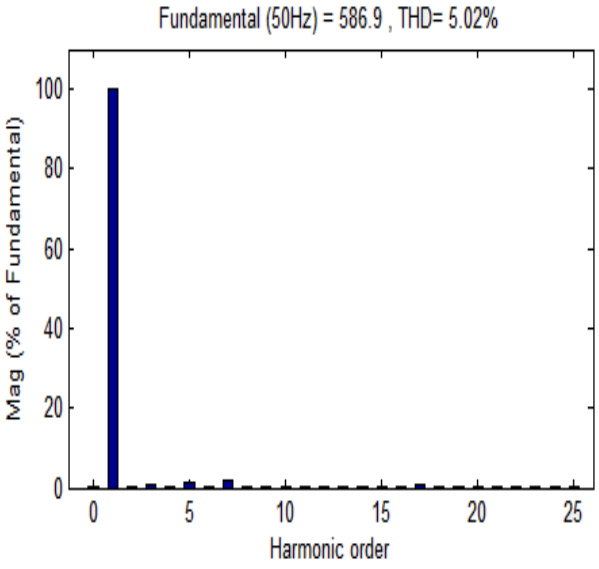


Fig. 14 Line voltage (V_{ab}) THD for PD Multicarrier - 60° PWM

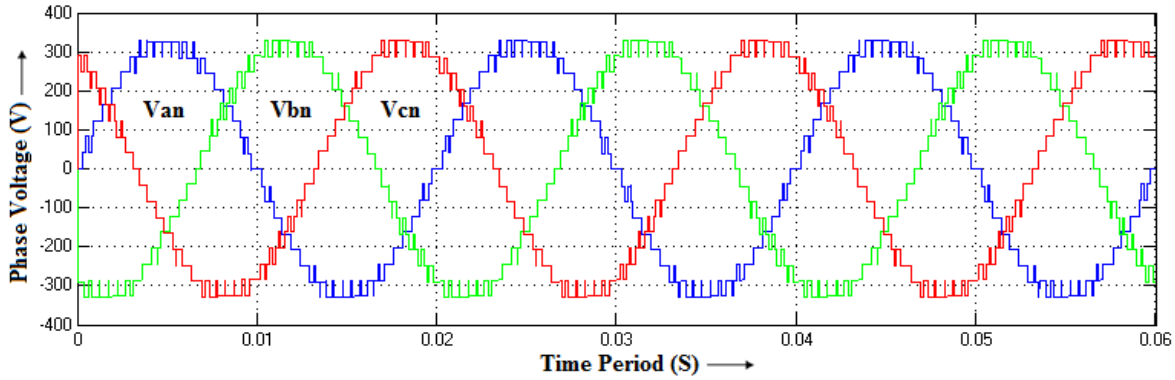


Fig. 15 *W*aveform for Phase voltage using PD MCPWM

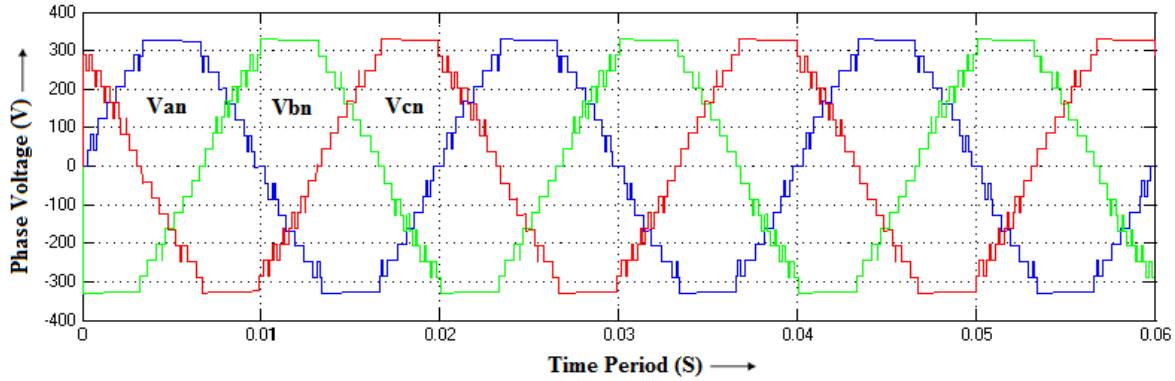


Fig.16 *W*aveform for Phase voltage using PD Multicarrier - 60^{o} PWM

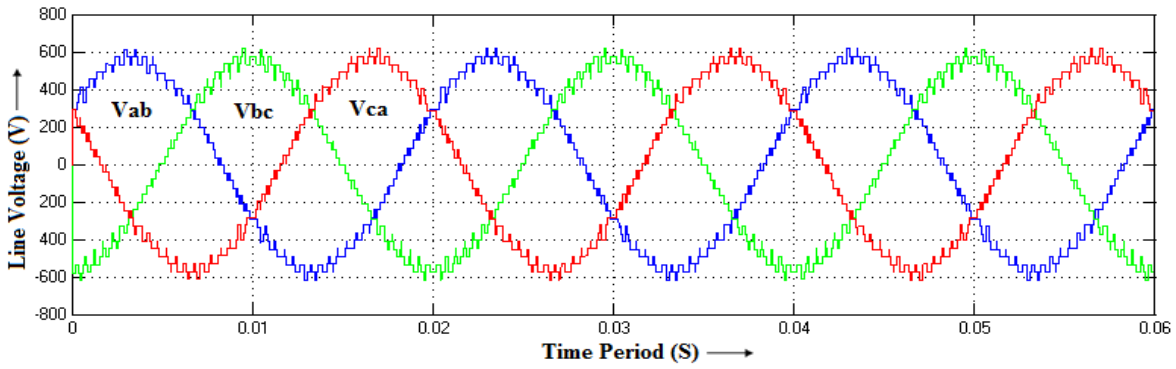


Fig. 17 Waveform for Line voltage using PD MCPWM

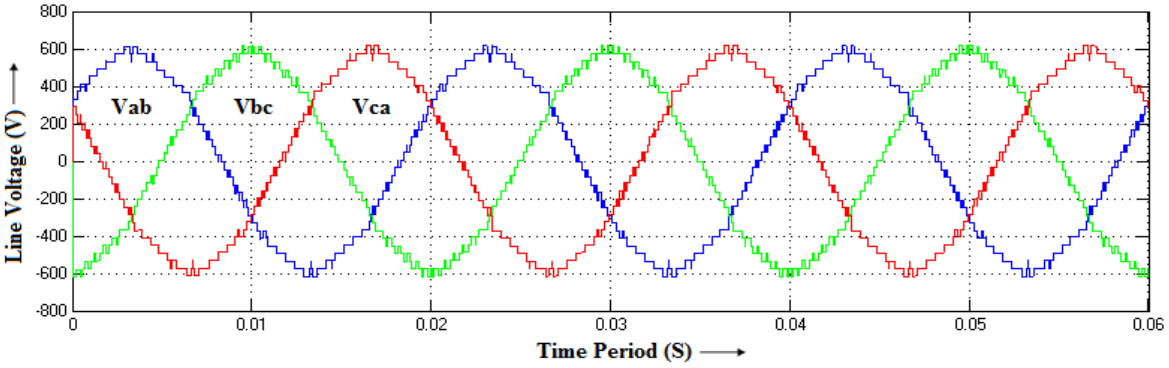


Fig. 18 Waveform for Line voltage using PD Multicarrier - 60^{o} PWM

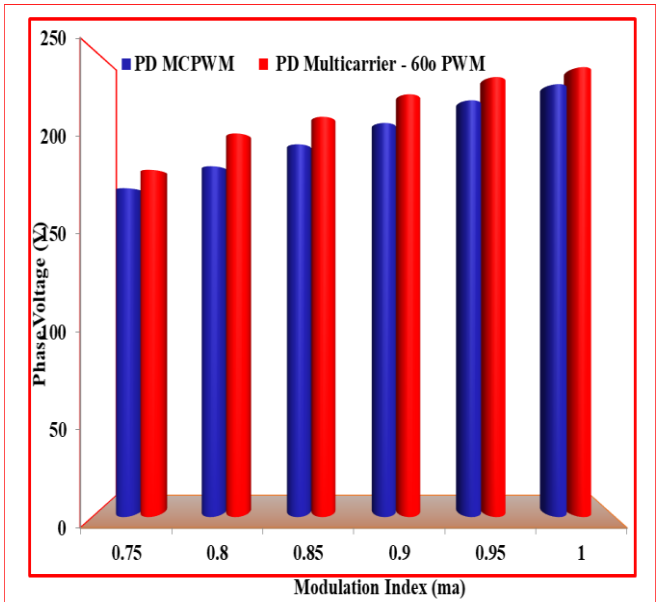


Fig. 19 Comparison of Phase Voltage with the variation of Modulation Index

Table 4 Comparison of line voltage with PD MCPWM and PD Multicarrier - 60° PWM

Modulation Index (m_a)	PD MCPWM		PD Multicarrier - 60° PWM	
	V_{ab}	THD (%)	V_{ab}	THD (%)
1	403.9	7.20	**415.1**	**5.02**
0.95	384.5	7.44	**404.2**	**5.54**
0.9	364.4	7.96	**380.4**	**5.92**
0.85	342.0	8.05	**354.3**	**6.41**
0.8	325.1	8.53	**334.9**	**7.13**
0.75	303.1	8.98	**313.5**	**7.51**

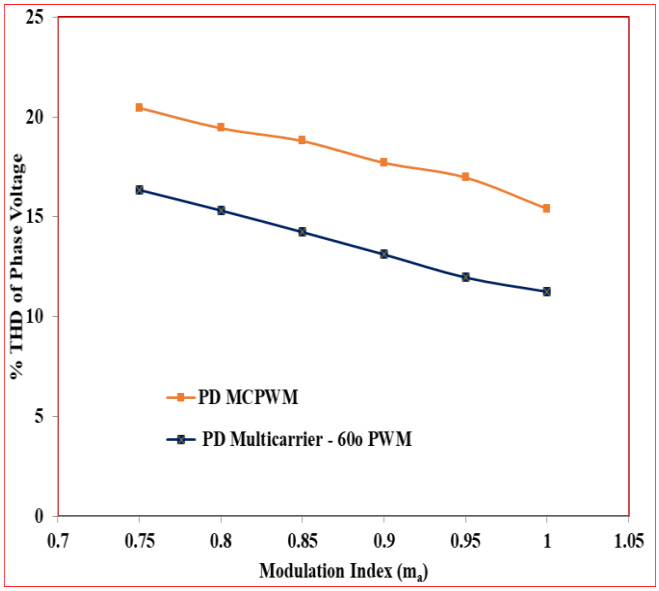


Fig. 20 Comparison of % THD of Phase voltage with the variation of Modulation Index

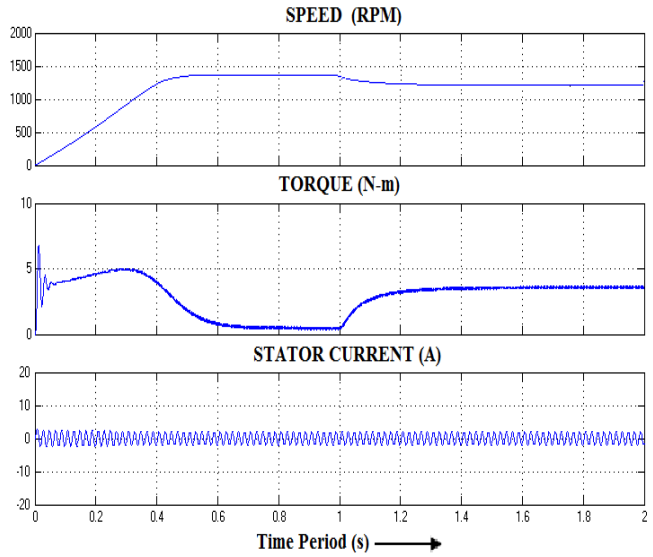


Fig. 21 Waveforms for speed (rpm), torque (N-m) and stator current (A) of the IM

The truth that the new PWM approach extracts almost the same fundamental output for the same operating point both using simulation and hardware with comparable THD values goes to validate the proposed formulation. The closeness of the entries in Table 5 over a range of operating loads further claim the use of the chosen topology and establish the reliability of the new PD Multicarrier - 60° PWM for MLI fed induction motor drives.

Table 5 Comparison of Simulation and Hardware Results using PD Multicarrier - 60° PWM

Load in Kw	V_{AB}		V_{BC}		V_{CA}		Speed (RPM)	
	SMN	*HW*	*SMN*	*HW*	*SMN*	*HW*	*SMN*	*HW*
0.1	415.1	413.7	415.0	413.4	415.1	413.5	1404	1398
0.2	415.1	413.6	415.0	413.1	415.0	413.6	1396	1391
0.3	415.0	412.3	414.9	412.8	414.9	412.1	1387	1382
0.4	414.9	411.7	414.9	411.8	414.6	411.9	1381	1374
0.5	414.7	411.4	414.8	411.6	414.3	411.3	1374	1366
0.6	414.6	411.4	414.7	411.4	414.1	411.4	1365	1359

SMN- Simulation, HW – Hardware

VII. CONCLUSION

A new asymmetrical three phase MLI has been conceived to produce a nearly sinusoidal variable voltage for operating a three phase IM. The two H-bridges with unequal dc voltage sources in each of them has been enlivened to follow a series parallel switched path for the flow of current . The methodology has been enabled on the guidelines of a new PWM scheme to foster an increase in the fundamental component of the stator voltage and an associated decline in its THD .

The performance over a various modulation indices has been examined through MATLAB-based simulation.
The results have been presented to determine the MLI's ability to generate higher levels of output voltage while simultaneously enjoying the formulation of the new PWM scheme for exploring fresh utilities to match the developing automated world.

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