International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9, Issue-7, May 2020

Analysis of Low Power Dynamic Comparator

M. Sai Navya, U. Koti Reddy, N. Yaswanth Kumar, G. Sai Krishna, P. Lakshman

Abstract: ***Low power consumption, high performance dynamic comparators are widely used in high-speed Analog to Digital Converters (ADCs) and advanced input/output circuits. Mostly unique comparators utilize the latching stage thorough cross-coupled inverters, which gives a solid positive feedback, to fasten the comparison and reduce the static- power dissipation. In this paper, the analysis of dynamic comparators having best performance parameters in terms of power dissipation is presented. This is achieved by adopting low power techniques like adding transistors and sizing them to get efficient circuit. The proposed circuits are able to reduce power dissipation from 40-50%.***

Index Terms: Dynamic Comparators, High performance, Low power, Delay, Analog-to-Digital.

I. INTRODUCTION

Comparators are most important basic building blocks in the Analog-to-Digital converters. Delay as well as consumption of power in the comparator plays the important role in the Analog-to-Digital Converter namely flash Analog-to-Digital Converters (ADCs) and successive approximation register (SAR). In the past mainly used comparators are Static comparators. But Static comparators consume more power and they are low in speed [1]. Therefore Dynamic comparators are came into picture to decrease the consumption of power and increase the comparison speed of the input signal voltage and reference voltage. In dynamic comparator the input signals are amplified in the pre-amplifier stage and the voltages to the vdd level as well as at the gnd level in the latch stage at that time. In dynamic comparator it uses strong positive feedback latch, in that positive feedback it gives a high comparison of speed of two differential input voltage signals by the latch. The dynamic comparators determines offset voltage, the speed and the power consumption through the pre-amplifier stage and the latch stages [2]. The high performance and consumption of low-power dynamic comparators are mostly used for high-speed Analog-to-Digital Converters (ADCs).

Revised Manuscript Received on May 30, 2020.
***** Correspondence Author
M. Sai Navya*, UG Student, Department of ECE, Koneru Lakshmaiah Education Foundation, Vaddeswaram, A.P , India.
U. Koti Reddy, UG Student, Department of ECE, Koneru Lakshmaiah Education Foundation, Vaddeswaram, A.P , India.
N. Yaswanth Kumar, UG Student, Department of ECE, Koneru Lakshmaiah Education Foundation, Vaddeswaram, A.P , India.
G. Sai Krishna, Associate Professor, Department of ECE, Koneru Lakshmaiah Education Foundation, Vaddeswaram, A.P , India.
P. Lakshman, Associate Professor, Department of ECE, Koneru Lakshmaiah Education Foundation, Vaddeswaram, A.P , India. Email: navya0507.movva@gmail.com,yaswanthnavale043@gmail.com, koti7578@gmail.com

Because of the input impedance is high, full output swing and there is no static consumption of power latch type amplifiers are mostly used in Analog to Digital converters. Because of the few stacked transistors high voltage headroom is needed for it to work properly which is the challenging task in the CMOS technology. Offset voltage and the structure speed is complex to input common mode voltage which isn't suitable for application with input common mode variations. Dual tail comparators has less stacking transistors, which makes it appropriate for low voltage applications. In dynamic comparator the latch stages and the pre-amplifier stage are separated to one another, which increase the speed of comparison and amplify the compared signals [3].

In the two stage comparator [4] the dynamic bias pre-amplifier at the internal modes it's partially discharges which decrease the consumption of power but the delay is greater than that of conventional design circuit. The additional positive feedback and clocking system in [5] are designed in the pre-amplifier stage to enhance gain at the pre-amplifier.

Mostly all the dynamic comparators uses cross-coupled latching stages to obtain high performance and low power. In [6], the delay and the power consumption are decreased with the help of trans conductance-enhanced latching stage. This paper, we give the power analysis and the delay analysis of the dynamic comparator simulated in a 0.13-μm CMOS. The proposed design and conventional design operates at 1.2-V supply.

II. BACKGROUND AND ANALYSIS

Conventional Dynamic Comparator:

Fig-1, represents with pre-amplifier and latching stage to the Conventional Dynamic Comparator. The pre-amplifier is used to produce an amplified difference between the two input signals and the latch is used for comparison. During the reset process when the CLK=0 and CLK^1=1, nodes D_N and D_P of the voltages charged to V_{DD} which causes output-nodes to discharge to V_{SS}.

In the evaluation phase, when CLK=0 to 1 and CLK^1=1 to 0, the pre-amplifier amplifies the differential voltage between the two input signals V_{INP} and V_{INN}. When the differential voltage is enough to drive the nmos, then latch starts working and takes the decision based on the input signals. In this conventional circuit design, the pre amplifier circuit consumes more power even after comparison is done. When the differential voltage is large (2 times or 1.5 times the V_{THN}), pre amplifier is wasting more energy than required.

$$t_{delay} = t_{latch} + t_0$$

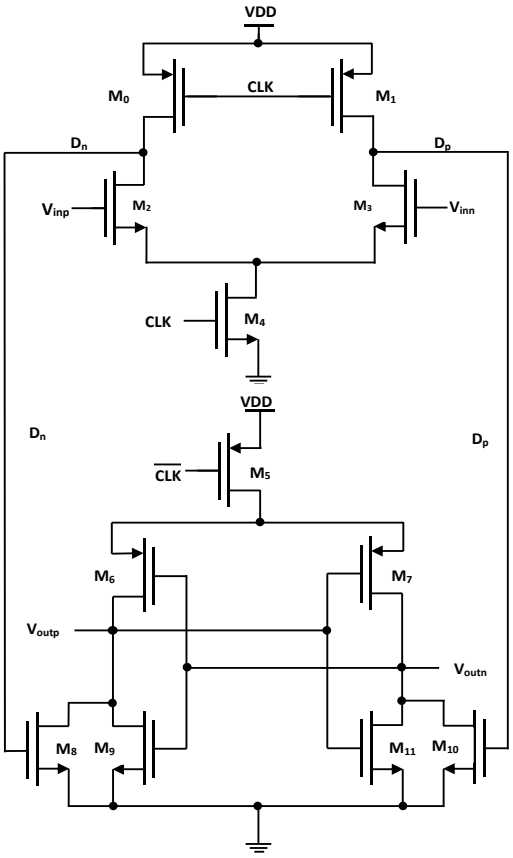


Fig-1. Conventional Dynamic Comparator

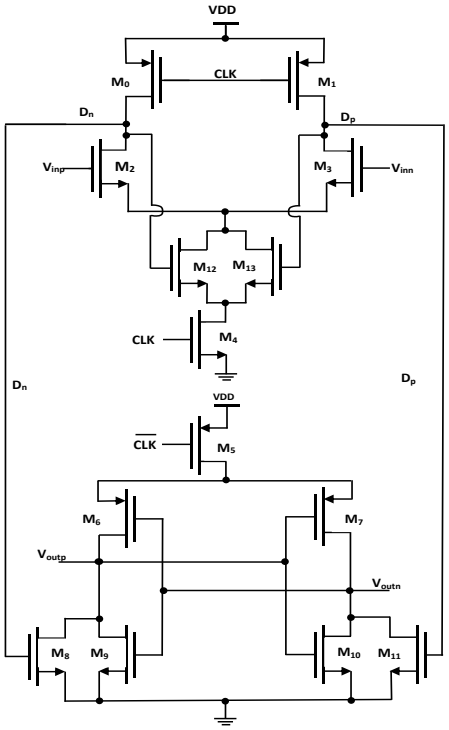


Fig-2. Proposed Cascade Dynamic Comparator

Fig-2, shows the Proposed Dynamic Comparator with two cascade transistors. The working of this circuit is the same to the Conventional Dynamic Comparator Fig-1. In this circuit design, the pre amplifier circuit is not capable of wasting more energy. In reality, while the output voltage of the pre-amplifier go near to $(|V_{DD}-V_{THN}|)$ (threshold voltage of M12-13) the tail current approaches zero without losing charge in the output nodes. When simulating the proposed design, the voltage supply should be very high so that $(|V_{DD}-V_{THN}|)$ is far greater than V_{THP}, so the latch is triggered strong at the comparison phase without a delay. Hence, the minimal voltage supply is fixed to V_{DD}- $(V_{THP} + 5*V_{THN})$.

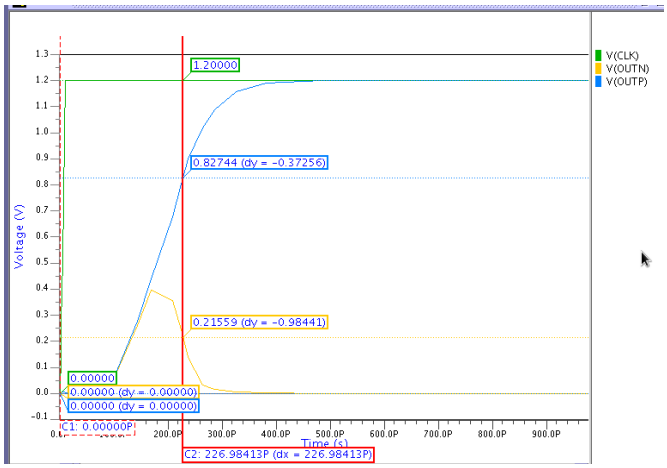


Fig-3. Waveforms of conventional dynamic comparator

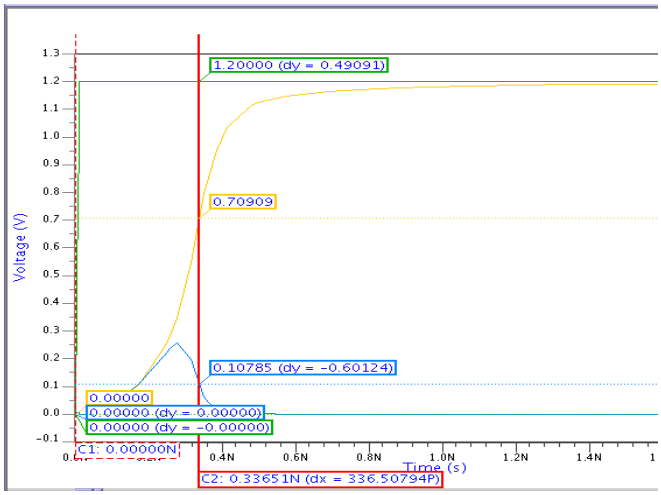


Fig-4. Waveforms of conventional dynamic comparator

Two-stage Dynamic Comparator with Cross Coupled latch:

Fig-5, Represents the two stage Dynamic Comparator with the pre amplifier and a cross coupled latch .*CLK1* signal is given a delay of 45ps from *CLK*. When *CLK=0* i.e. in the reset phase, nodes D_N and D_P are charged to *VDD*, M5,M6,M9,M12 are charged, M7,M8 are off. Through transistors M9-12, B_N and B_P nodes are discharged to *GND* and *Voutp*, *Voutn* are charged to *VDD* through transistors M5, M6.

The other cross coupled design circuits triggers the strong inversion region by only two transistors and other transistors in cut-off region in the reset phase where as in this circuit M5,M6,M10 and M11 are set to be triggered in the strong inversion region. In evaluation phase, this circuit has higher trans conductance than the Fig-1, Fig-2, which enhances the comparison speed.

Energy consumption can be reduced by faster comparison which ends with the stable state of inverters in latch. *CLK1* is given with a delay of t_{opm}, so that M0 and M1 are on in order to remove short circuit path through M9 and M12 when *CLK moves* from 0 to1.

$$t_{delay} = t_{omp} + t_{latch} + t_0$$

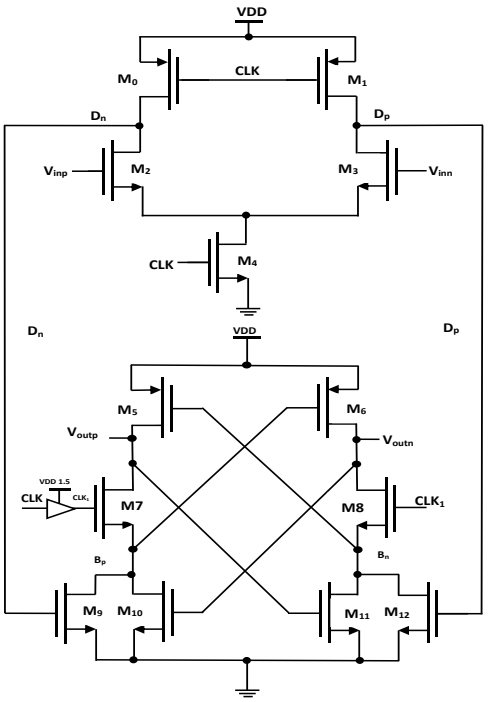


Fig-5. Conventional Dynamic Comparator with Cross Coupled latch

In order to reduce delay in Fig-1, A Dynamic Comparator with cross coupled latch is implemented. Delay can be reduced by enhancing the total trans-conductance of the circuit through new latching stage, especially for t_0 when the operation enters the evaluation phase.

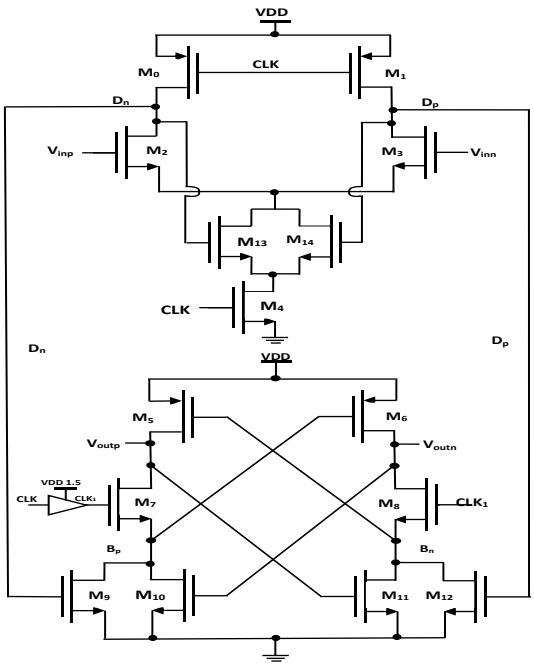


Fig-6. Proposed Cascade Dynamic Comparator with cross coupled latch

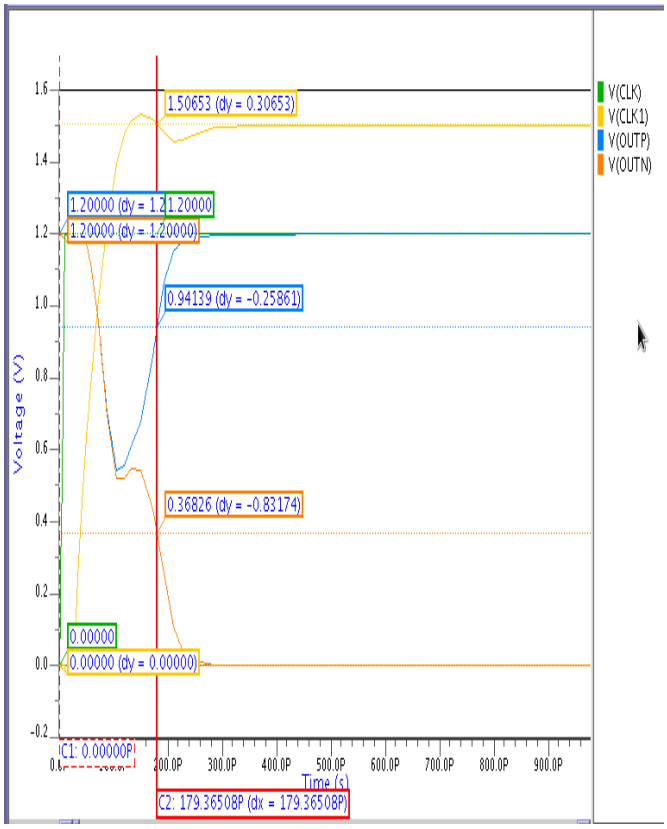


Fig-7. Waveforms of Proposed Cascade Dynamic Comparator with cross coupled latch

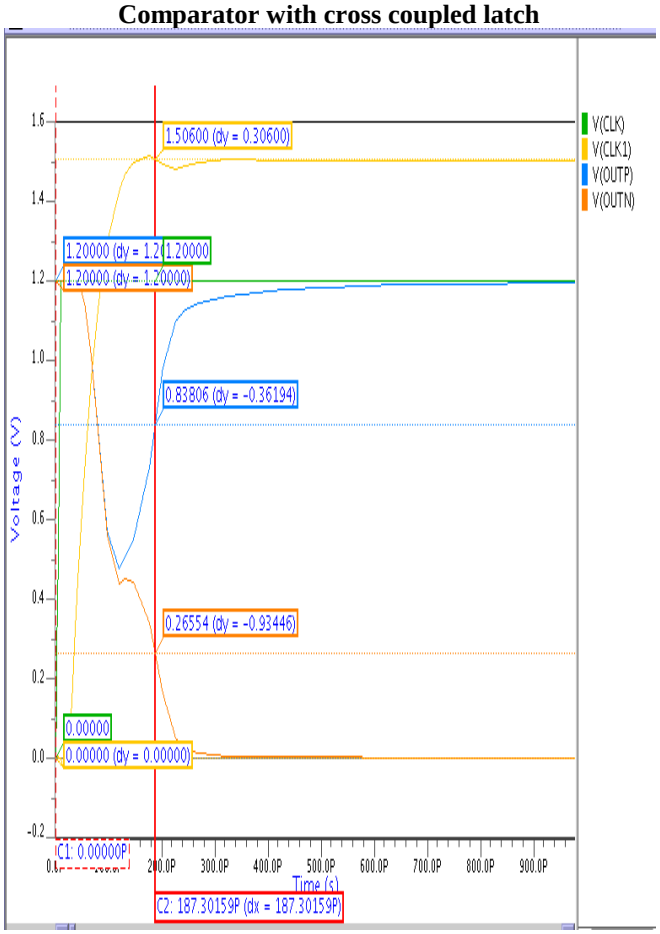


Fig-8. Waveforms of Proposed Cascade Dynamic Comparator with cross coupled latch

Table-1: Comparison between conventional and proposed dynamic comparators

Comparator	Delay(ps)	Power(nW)	Offset(mV)
Conventional dynamic comparator	226.1	4.07	7.11
Proposed cascade dynamic comparator	336.5	1.97	7.11
Conventional dynamic comparator with cross coupled latch	179.6	7.107	7.3
Proposed cascade dynamic comparator with cross coupled latch	187.30	4.637	7.3

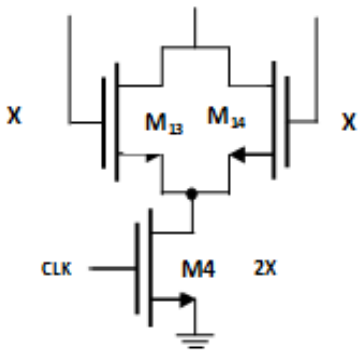
Dimensions of Proposed Cascade Dynamic Comparator with cross coupled latch:

Transistor ID	Size of transistor(μm)
M0,M1	0.5/0.13
M2,M3	4.0/0.13
M4	0.44/0.13
M5,M6	2.0/0.13
M7,M8	1.8/0.13
M10,M11	1.0/0.13
M9,M12	2.0/0.13
M13,M14	0.44/0.13

III. RESULTS AND DISCUSSION

Pre layout simulations reveals that the proposed dynamic comparators are efficient to reduce power dissipation in dynamic comparators. Table1 shows the comparison between the conventional and proposed dynamic comparators. The proposed design is the simplest way to achieve lower power values as we adopted transistor sizing as low power technique. The newly added cascade transistors are changed with their widths to achieve reduced power values.

Table-1 depicts that the proposed cascade dynamic comparator reduces the power dissipation by 50% compared to conventional dynamic comparator with an offset of 7.11mV and frequency of 510MHz where as the proposed cascade dynamic comparator with cross coupled latch reduces the power dissipation by 35% compared to conventional dynamic comparator with cross coupled latch with an offset of 7.3mV and frequency of 510MHz.



IV. CONCLUSION

In this paper, we observed power dissipation of proposed and conventional dynamic comparators in 130nm technology. The power of Cascade proposed dynamic comparators are seen with varying widths of cascade transistors (M13, M14) in 130nm. We got minimum power dissipation of proposed dynamic comparators when width of cascade transistors is 0.44nm. Hence the proposed dynamic comparators are efficient than conventional comparators.

REFERENCES

1. Y. Wang, M. Yao, B. Guo, Z. Wu, W. Fan and J. J. Liou, "A Low-Power High-Speed Dynamic Comparator With a Transconductance-Enhanced Latching Stage," in *IEEE Access*, vol. 7, pp. 93396-93403, 2019.
2. Razavi, B, and Wooley, "Design techniques for high-speed, high resolution comparators", IEEE J. Solid-State Circuits, 1992, 27, (12), pp. 1916–1926.
3. A. Khorami, M. Sharifkhani, "A low-power high-speed comparator for precise applications", *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 10, pp. 2038-2049, Oct. 2018.
4. D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time,"in 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, Feb 2007, pp. 314–605.
5. H. S. Bindra, C. E. Lokin, A. J. Annema, and B. Nauta, "A 30fJ/comparison dynamic bias comparator," in Proc. IEEE European Solid State Circuits Conf.(ESSCIRC), 2017, pp. 71–74.
6. T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW pipeline A/D converter," in *IEEE Journal of Solid-State Circuits*, vol. 30, no. 3, pp. 166-172, March 1995.
7. A. Khorami, M. Sharifkhani, "High-speed low-power comparator for analog to digital converters", *AEU—Int. J. Electron. Commun.*, vol. 70, no. 7, pp. 886-894, 2016.
8. A. Khorami, R. Saeidi , Manoj S, M. Sharifkhani,"A low-power dynamic comparator for low-offset applications", Integration, the VLSI Journal 69 (2019) 23–30.