International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9, Issue-7, May 2020

VLSI Implementation of Linear Feedback Shift Register (LFSR) based Test Pattern Generator for Pseudo Exhaustive Testing

S. Sridhar, K. Mounika, M. Anjali, G. Venkatesh, M. Murali Krishna

Abstract: ***Advanced strides of improvement in programmable logic density, enhancements in speed and hardware description language (HDL) are empowering design engineers to implement highly performing and testable digital systems. Linear feedback shift registers (LFSR) are the critical elements in the testing and self testing of contemporary complex electronic systems like processors, Built-in-self-test (BIST) controllers and integrated circuits (ICs) etc. Fundamentally BIST is a Design-for-Testability (DFT) technique meant to configure testing functions physically with the circuit under test (CUT). To enhance the percentage of fault coverage as a part of BIST operations (testing the IC), LFSRs are deployed (as test pattern generator) to generate the test vectors inside logic BIST for testing digital systems. Proposed work is focused upon designing a fast adder based variable length pseudorandom binary sequence pattern generator (PRBSPG) and experimental validations. LFSR possess characteristics of high speed, better encoding efficiency, high fault coverage, low test volume data and low power consumption specially suitable in processing environment where uniform distribution random numbers are required. Verilog HDL is employed for structuring the modular design units while Xilinx ISE tool is deployed for validating the proposed LFSR design work and associated modular units.***

Keywords: Xilinx ISE, Verilog HDL, BIST, DFT, LFSR.

I. INTRODUCTION

Effective testing mechanisms ensures correctness of design to determine whether the device meets all specifications are not. Testing plays a significant role in digital systems to verify the functionality, performance, reliability and usability of any product or software application. VLSI testings are meant to verify the design correctness and detect all parametric faults, random defects in the manufactured chips[1].

Revised Manuscript Received on May 30, 2020.
***** Correspondence Author
Siripurapu Sridhar*, Professor, Department of Electronics and Communication Engineering, Lendi Institute of Engineering and Technology, Vizianagaram, India.
K.Mounika, B. Tech, Department of Electronics and Communication Engineering, Lendi Institute of Engineering and Technology, Vizianagaram, India.
M. Anjali, B. Tech, Department of Electronics and Communication Engineering, Lendi Institute of Engineering and Technology, Vizianagaram, India.
G. Venkatesh, B. Tech, Department of Electronics and Communication Engineering, Lendi Institute of Engineering and Technology, Vizianagaram, India.
M. Murali Krishna, B. Tech, Department of Electronics and Communication Engineering, Lendi Institute of Engineering and Technology, Vizianagaram, India.

Built-in-self-test (BIST)or built-in test (BIT) epresents a kind of on-chip testing mechanism that permits a machine to test itself. Engineers design BISTs to meet requirements of high reliability and lower repair cycle times.

BIST is a technique of designing additional hardware and software features into Integrated Circuits (ICs) allowing them to perform self-testing, i.e., testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external automated test equipment (ATE). BIST mechanisms are predominantly deployed in medical devices, automative electronics, avions, weapons, complex and unattended machinery of all types and integrated circuits. BIST is a kind of Design-for-Testability (DFT) technique that ensures testing of critical circuits having no direct connections to the external pins such as embedded memories. It simplifies electrical testing of chips fastly and efficiently in a more economical manner. The concept of BIST can be applied to just about any kind of circuit where its implementation varies widely in accordance with the product diversity it caters to. As an example, a common BIST approach for DRAM's includes the incorporaing on-chip additional circuits for pattern generation and go-/no-go diagnostic tests.

Testing through BIST involves storing one of the good test patterns in an on chip ROM, applying test patterns to the CUT and obtained responses are compared with the respective stored patterns. Based upon the implementation and performance mechanisms ,there are several specialized versions of BIST like logic BIST,programmable BIST etc. Built in Self Test mechanisms basically generate test patterns or test vectors to detect faulty operations of the designs under test (DUT)[6]. The components of BIST include Pseudorandom Binary Sequence Test Pattern Generators (PRBSG or PRBSTPG) that apply a sequence of test patterns to the Circuit Under Test (CUT)[10]. PRBS generator is mostly implemented using a linear feedback shift register (LFSR). LFSR can be used to both generate the required binary test patterns sequence for the design (or circuit) under test[4] and also capture the response of design and generate a signatur (the bit pattern held in the signature register). In comparioson with binary counters, LFSR's are more efficient for test pattern generation in order to improve the fault coverage[5][6], LFSR's can generate maximum length sequence[1]. In logic circuits, functional tests generated by LFSRs can cover high percentage of modeled faults[2][7].LFSR reseeding is dynamic and it allows partial reseeding.For better encoding efficiency, partial dynamic LFSR has some simple hardware implementation than other multi polynomial LFSR[9].This partial LFSR reseeding can help to reduce the test data storage and bandwidth[8][3].

Different methodologies of implementing LFSRs are discussed in section II, while the proposed LFSR architecture is elaborated in section III. Experimental evaluations and analysis are described in section IV and section V concludes the manuscript.

II. METHODOLOGY

Shift Registers are used for data storage and for data movement as well, they are commonly used inside calculators or computers to store data and to convert the data from either serial to parallel or parallel to serial format etc. Shift registers are built up of Dflipflops connected in series. The number of bits stored in the registers is directly proportional to the number of flip flops it is made up of. LFSR is a shift register whose input is linear function of previous state, its design is very simple and easy to implement. LFSR's are made up of D-flip-flops and XOR gates, In shift registers, we can predict the next value. Where as in LFSR's, we cannot predict the next value. An LFSR is used to generate different pseudo random patterns by changing the "seed" value. The maximum length of seed value is:2n-1.In LFSR,the test pattern will repeat after 2n-1 clock cycles. For example,4-bit seed can generate 15 pseudo random patterns.In 16th clock pulse again the pattern will repeat. Different types of LFSRs are discussed ahead. Figure.1 below shows an 8 bit LFSR.

This LFSR is like a black box which generates an output that is a linear function of the input (typically created by a combination of shifting, and Exclusive-OR, of the bits) on feeding a number.

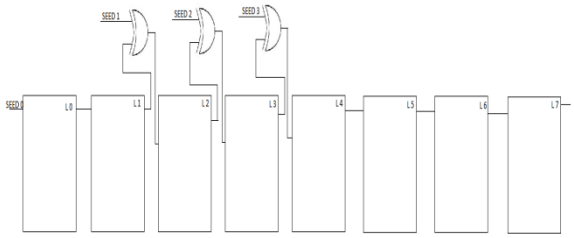

Fig1: 8-Bit LFSR

Architecture of Fibonacci type LFSR is discussed in Figure.2 below. The bits which will affect the next state as the inputs are called as Taps.Here the taps are 16,14,13 and 11. Here the rightmost output bit is XORed with the tapped position bits and given as feedback to the leftmost bit. XNOR gates can also be used instead of XOR gates, however XNOR operation results in complemented values of LFSR states. The state with all Ones using XNOR gates and the state with all zeros using XOR gates represent the "locked-up" or invalid state.

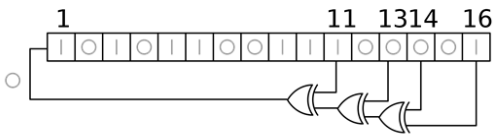

Fig2: Fibonacci LFSR

Architecture of Galois type LFSR is elaborated in Figure.3 below. This Galois LFSR is lmost same as LFSR.If the system is locked, the bits which donot have taps will shift by 1-bit to the right position without any change.If they have taps, they will be XORed with the output bit before moving to the next position.

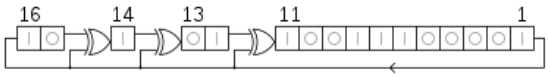

Fig3: Galois LFSR

Now, the output bit is the input bit, if the output bit is zero, the register contents are shifted right without any change in bits and input becomes zero. Similarly if the output is one, the bits will be flip which are in tap positions and the bits will be shift to right and input will become one. In Galois LFSR, the speed execution keeps on increasing because the bits do not combine at every tap to attain new input .Galois LFSR is very easy to implement in software..

LFSRs can also be expressed in Matrix forms. Column vector (a0,a1…….an-1)T is the seed. Pseudo-random sequence can be generated by using the hardware of LFSR.

$$\begin{pmatrix} a_k \\ a_{k+1} \\ a_{k+2} \\ \vdots \\ a_{k+n-1} \end{pmatrix} = \begin{pmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ c_0 & c_1 & c_2 & \cdots & c_{n-1} \end{pmatrix} \begin{pmatrix} a_{k-1} \\ a_k \\ a_{k+1} \\ \vdots \\ a_{k+n-2} \end{pmatrix} = \begin{pmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ c_0 & c_1 & c_2 & \cdots & c_{n-1} \end{pmatrix}^k \begin{pmatrix} a_0 \\ a_1 \\ a_2 \\ \vdots \\ a_{n-1} \end{pmatrix} \quad (1)$$

LFSR's can also be employed as counter having high clock rate. LFSR are used in cryptography (due to simple construction), communication, scrambling and broadcasting applications etc.

III. PROPOSED ARCHITECTURE

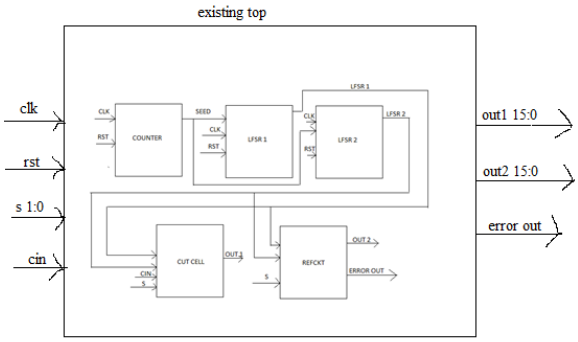

Fig4:Block Diagram

The proposed architectural implementation (Shown in Figure.4 below) of LFSR design includes the design and validation of different modular units namely (for the design purpose)

A) Cut cell unit,
B) Counter unit,
C) LFSR unit and
D) Refckt unit respectively.

A.Cut cell consists of four inputs in which two inputs are from lfsr unit of 8bit ,cin of 1 bit size and selection line s is of two bit size.The selection lines are used to get the 16-bit output which is the output of cut cell. If the input of the selection lines is 01, the output will be 16-bit of the cut cell which is called as out1.Otherwise it will be sum of the addersub block.

Block diagram of Cut cell is shown in Figure.6.

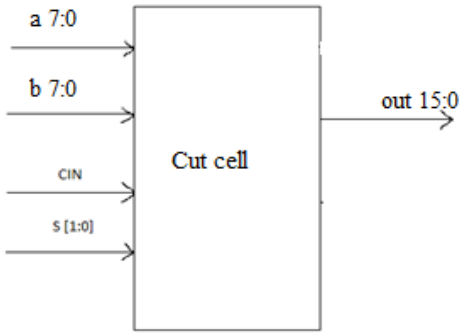

Fig5:Cut cell

Fig6:Tree Diagram

Architecturally Cut cell unit includes different sub modules like

I) Adder – subtractor unit and

II) 8-bit Vedic unit (Vedic8-bit).

Adder – subtractor unit inturn contains one bit adder-sub unit and full adder unit respectively.While the **Vedic8-bit unit** contains i) Vedic4-bit unit, ii) Vedic 2-bit unit and iii) Adder3-4 bit unit etc.

Further **Vedic 4-bit unit** consists of an adder 8-bit unit.**Vedic 2-bit unit** consists of AND gate and mod full.Adder 3-4 bit consists of mod full units respectively.

I) a)Adder-subtractor unit:

It contains of three inputs a,b,cin of size 8bit,8 bit and 1 bit respectiveky.The outputs are sum and Cout.sum is of size 8bit and Cout is of size 1-bit.It can perform both addition and subtraction at a time depends on control signal.

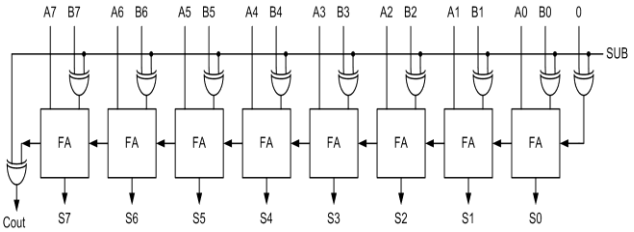

Fig7:Adder-subtractor

b)full adder:

Full adder contains three inputs a,b,c which are of 1-bit size.It has two outputs sum and carry.It will add the three bits at a time.

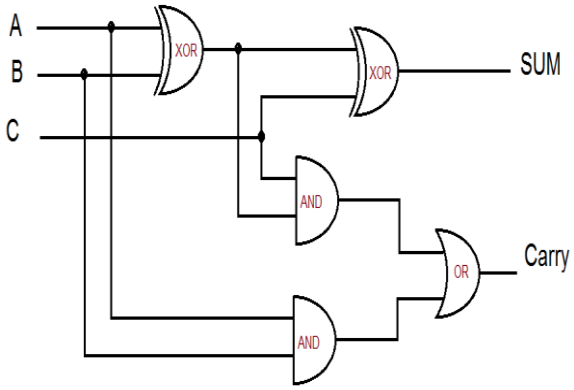

Fig8:Full Adder

II) Vedic 8 bit unit:

Vedic 8-bit contains input of 8-bit in which it contains two 4-bit sequences.It is employed by four Vedic 4-bit multipliers.It contains three adders.The first LSB bit will come normally.The next two multipliers output will be added at adder 1 and adder 2.The lastmultiplier output will be come from the adder3.

Here Vedic 8-bit multiplier contains two 8-bit inputs,one cin.The output is of 16-bit.

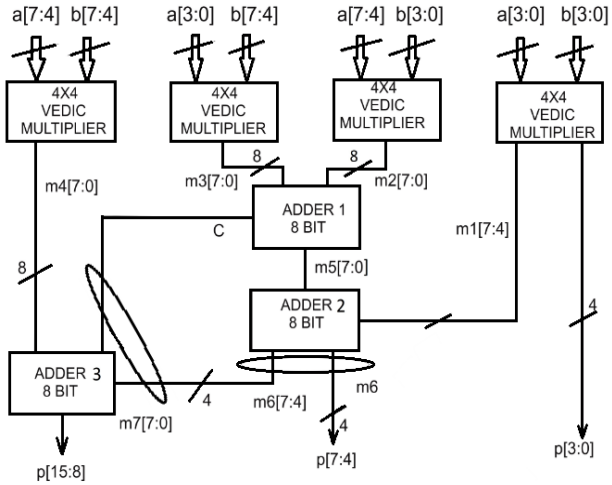

Fig9:8 –Bit Vedic Multiplier

a)Vedic 4-bit multiplier:

It has four 2-bit Vedic multipliers.Each multiplier will have two bits of input .They will multiply the bits and add to the ripple carry adder then wewill get the output of 8-bit.

Here Vedic 4-bit contains two inputs of size 4-bit and one cin.The output is of size 8-bit.

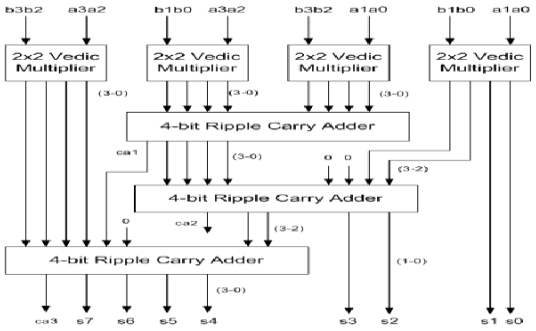

Fig10:4 –Bit Vedic Multiplier

i)Adder 8-bit:

It takes input of 4-bit and one cin.The output of first adder co is givn as input to the next adder.Here adder 8-bit contains input of two 8-bits and one cin.Outputs are s is of size 8-bit and ca is of size one bit.

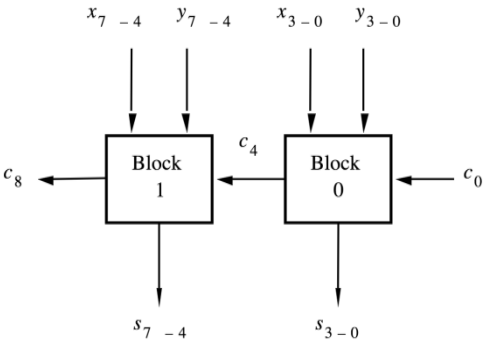

Fig11:8 Bit Adder

b)Vedic 2-bit :

Vedic 2-bit multiplier contains two inputs of size two bits.Firstly,the two LSB's will be multiplied.The carry will go to the next level.In next level. the crosswiseoperation will be performed.The carry will go to the MSB.The MSB's of two numbers will be multiplied.The output will be of 4-bit.

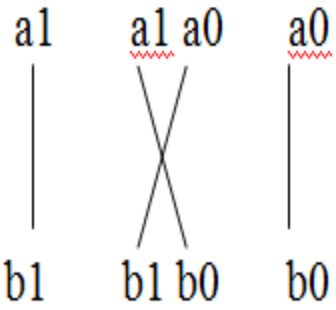

Fig12:2 –Bit Vedic Multiplier

Here, to perform 2-bit multiplication we will use andgate and mod full.

i)And gate :

When the both inputs are 1,the output will be 1.Otherwise ,the output will be 0.

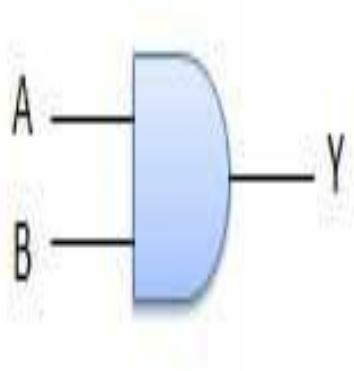

Fig13:AND Gate

ii)Mod full:

It contains three inputs a,b,c and two outputs sum and carry.

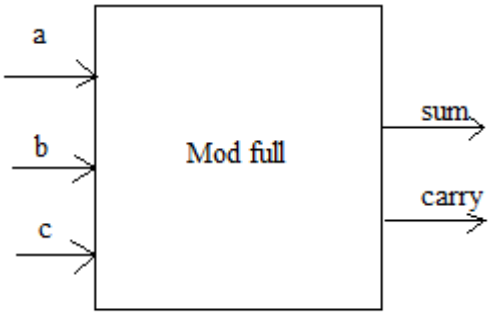

Fig14: MODFULL

c)Adder3-4 bit:

It consists of two 4-bit inputs and one c1.It is employed by four full adders.The sum will be taken at every full adder and carry will be forwarded to the next full adder.The output will 4-bit one cout.

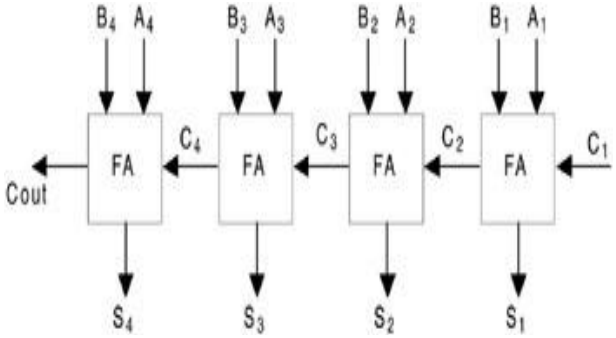

Fig15:Adder3-4 Bit

Here adder 3-4 bit contains two4-bit input and one cin.The output will be 4-bit and cout.It also contains mod full module.

B)Counter unit:

Counter unit (Shown in Figure.6) consists of clk, rst, clk edge of the counter should be always positive. Output of the counter is 4-bit known as the seed value.

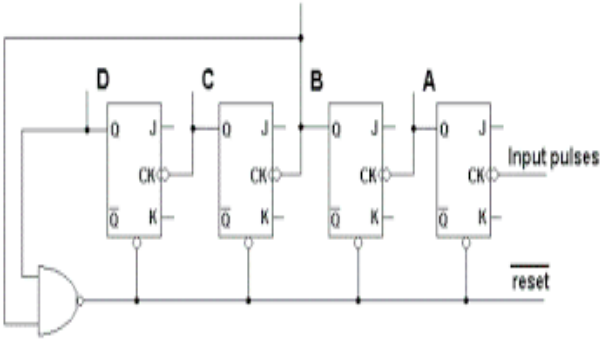

Fig16: Counter

Output of the counter is given to LFSR as input.

C)LFSR unit:

Here the proposed system consists of two LFSR circuits. Each of input size 4-bit and output size 8-bit. Here we have taken an 8-bit lfsr and three XOR gates, 4bit input and positive edge clk (D-flip-flops are used). 8bit output values are from L0 to L7. L0 value is same as input seed LSB bit.L0 value will pass to L1 register.

The output of L1 and seed value of second bit is given to XOR gate.The output of XOR gate will pass to L2.The output of L2 and seed value of third bit will undergo XOR operation.The output of XOR gate will pass to L3. L3 output and seed value of MSB bit will undergo XOR operation.The output of XOR gate will pass to L4 register and soon upto L7.The output will be 8-bit.
For example, if the value of seed is 1000 for a positive edge clk, the output of lfsr is 11110000.

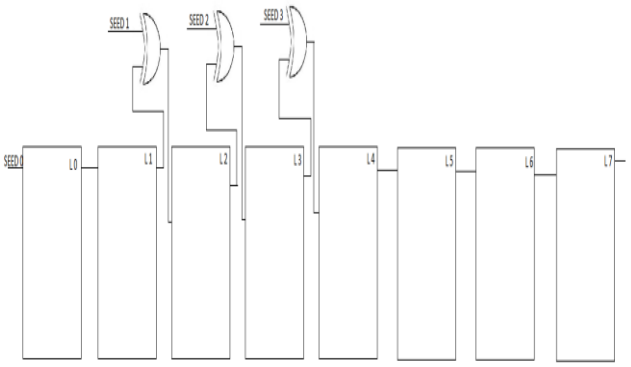

Fig17: 8-Bit LFSR

The outputs of LFSR1 and LFSR2 are given as input to the cut cell and ref ckt.
D) Ref ckt:
The refckt consists of three inputs which comprises of two 8-bit and one 2-bit .The output will be 16-bit.

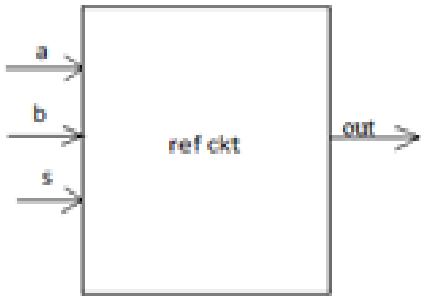

Fig18:refckt

Same LFSR1 and LFSR2 outputs and selection lines which is of 2-bit are given as input to the refckt. The output of the refckt is of size 16-bit which is called as out2.The selection lines are used to get the 16-bit output. If the input to selection line is 00, it will get sum of the input bits. If the input is 01, it will get multiplication of input bits. Otherwise it will get subtraction of the input bits.
Existing top:
Above are the submodules of the proposed system.These all modules are integrated in single block called existing top.
The existing top consists of inputs clk, rst, 1-bit value and 2-bit value.Always the clk should be positive edge and if rst is 1, then output will be 0000.Otherwise output will be 0001.The main module existing top has three outputs. They are out1, out2 and errorout.out1, out2 are the outputs of cut cell and refckt. Error out, if out1 is equal to out2 then output is zero. Otherwise it will be one.

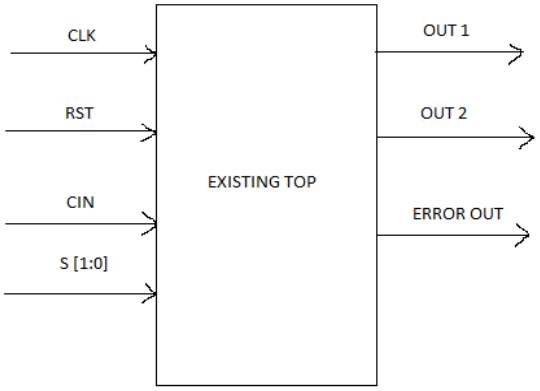

Fig19:Existing Top

IV. EXPERIMENTAL ANALYSIS

Counter contains the input clk and rst.Output is of 4-bit which is called as seed.The counter unit waveform is shown below

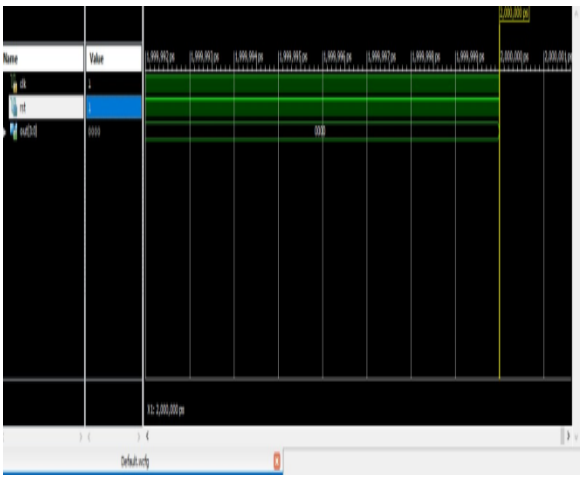

Fig20: Counter

LFSR1 and LFSR 2 contains the input of clk , rst and 4-bit .The output will be of 8-bit and it given to cut cell and ref ckt as inputs.The below are the waveforms of LFSR1&LFSR 2.

Fig21: LFSR1

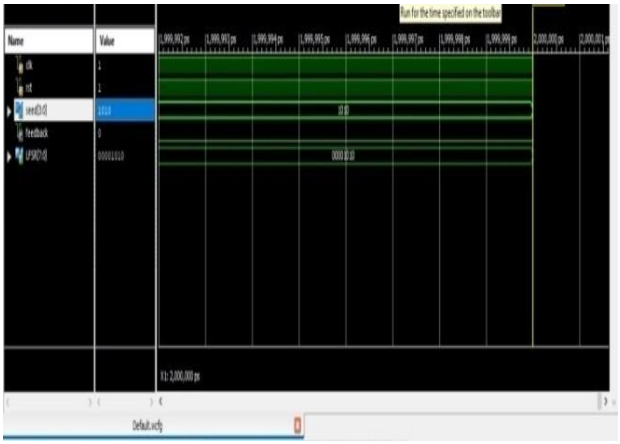

Fig22: LFSR2

Cut cell contains two 8-bits which are the outputs of lfsr1& lfsr2 ,cin of 1 bit size and s of size 2-bit as inputs and we get 16 bit output .The below fig is the waveform of cut cell unit.

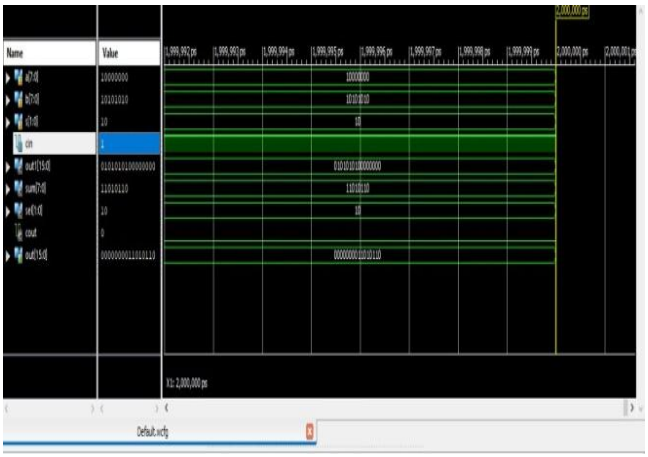

Fig23: Cut cell

Adder subtractor contains two 8-bit and cin as input and one 8-bit and cout as output.The below fig shows the simulation waveform of adder subtractor.

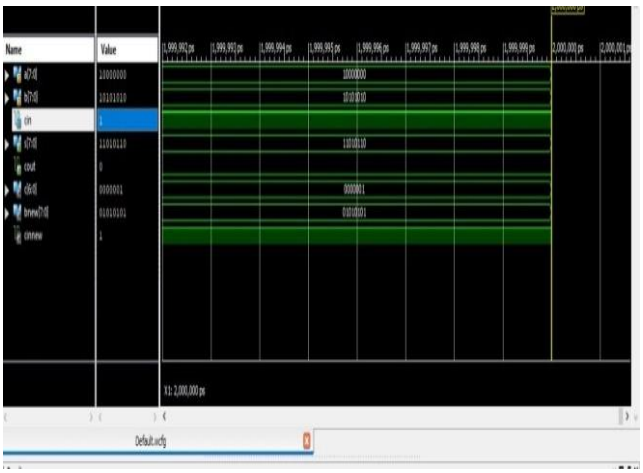

Fig24: Adder-Subtractor

Full adder contains three inputs a,b,c which are of size 1-bit and outputs are sum and carry. The below fig is the simulation waveform of full adder.

Fig25: Full Adder

Vedic 8 bit contains two 8-bit and one cin as input.Output is 16-bit.The below fig is the simulation waveform of Vedic 8 bit unit.

Fig26: Vedic-8 Bit

Vedic 4 bit contains two 4-bit and cin as input.Output is 8-bit.The below fig is the simulation waveform of Vedic 4 bit unit.

Fig27: Vedic-4 Bit

Adder 8 bit contains two 8-bit and cin as input .Output s is of size 8-bit and ca.The below fig represents the simulation waveform of adder 8 bit.

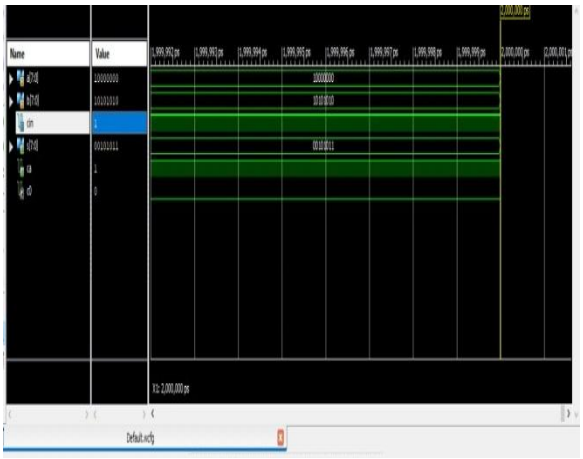

Fig28: Adder-8 Bit

Vedic 2 bit contains two 2-bit as input.Output is 4-bit.The below fig is the simulation waveform of Vedic 2 bit.

Fig29: Vedic-2 Bit

And contains two inputs and one output.The below fig shows the simulation waveform of and gate.

Fig30: AND

Mod full contains three inputs a,b,c.Outputs are sum and carry.The below fig shows the simulation waveform of mod full.

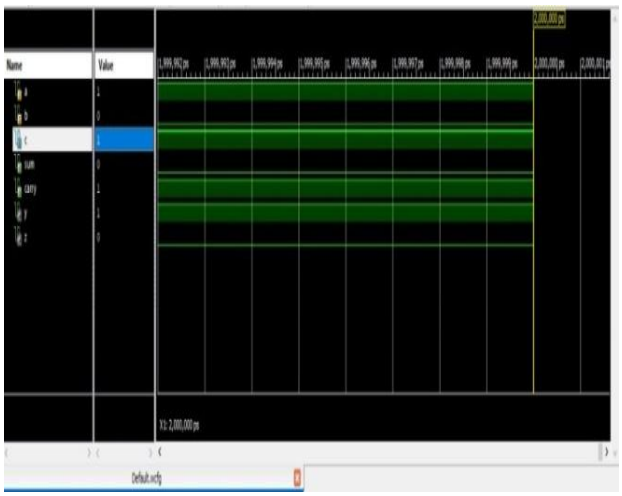

Fig31: Mod Full

Adder 3-4bit contains two 4-bit and cin as inputs.Output is 4-bit and co.The below fig shows the simulation waveform of adder 3-4 bit.

Fig32:Adder 3-4Bit

Ref ckt contains two 8-bit and one 2-bit as input.Output is 16-bit.The below fig shows the simulation waveform of the ref ckt.

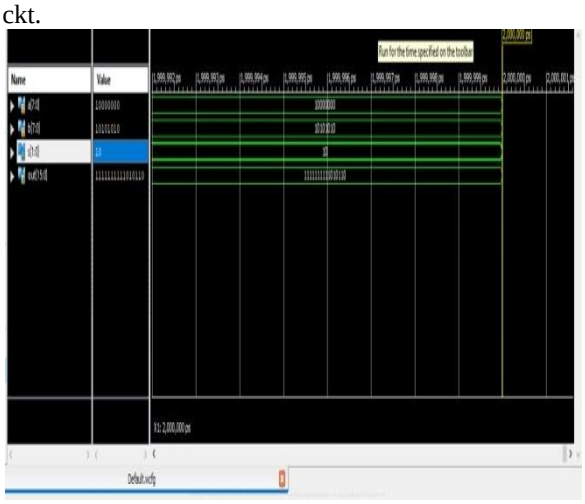

Fig33: Refckt

Existing top contains clk,rst,cin and one 2-bit as input.Outputs are out1&out2 of size 16-bit and an error out. Figure below represents the simulation waveforms of existing top level design.

Fig34:Existing Top

Parametric synthesis vaues relevant to 4-bit and 8-bit LFSR designs for BIST - implemented on SPARTAN3 XC3S700A FPGA device are tabulated below.

Table-I: Parametric Values

Parameter of Performance	4-Bit	8-Bit
Number of Slices	3	5
Number of Flip-Flops	4	8
Number of LUTs	4	8
Number of Bonded IOBs	7	15
Power Consumption (nW)	2452	4989
Max Frequency of operation(GHz)	491.673	510.89

Experimental values concerning 4-bit and 8-bit LFSR test pattern generator for BIST are promisingly good with regards to gate count, LUTs consumed and power consumption as discueed.

V. CONCLUSION

Testing of digital systems is spinning out to be more complicated keeping in view the enhancing scale of integration as predicted by Gordon Moore. An 8-bit reconfigurable PRBSG LFSR design for logic BIST architecture is presented in the manuscript to generate pseudorandom test patterns, proposed design ensure self testing of the CUT by detecting random pattern testable faults. Flexibility is incorporated in the design by having multiple tap insertion points to XOR gates added at the inputs of flip-flops based on the number of primary outputs to be generated. Reseeding ensures minimization of test length and complete fault coverage. Experimental evaluations depicted efficiency relevant to the execution speed as well as gate count utilization. Proposed LFSR technique can be enhanced further to generate more number of test vectors by having more number of varying sized inputs and inserting more tap points to ensure more better fault coverage and low volume of test data of course with incorporating additional hardware features.

REFERENCES

1. N. Devika, K Bhakthavatchalu, Ramesh. (2017). “Design of reconfigurable LFSR for VLSI IC testing in ASIC and FPGA.” 0928-0932.10.1109/ICCSP.2017.8286506.
2. Varghese, , Leeba, and G. Suranya. “Test Pattern Generation Using LFSR with Reseeding Scheme for BIST Designs.” International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering 3.5(2014): 452-458.
3. Kalaiselvi. M. and K. S. Neelukumari. “LFSR-reseeding scheme for achieving test coverage.” Information Communication and Embedded Systems (ICICES), 2013 International Conference on. IEEE, 2013.
4. Lai, Nan-Cheng, and Sying-JyanWang. “A reseeding technique for LFSR-based BIST applications” .Test Symposium, 2002.(ATS’02).Proceedingsofthe11thAsian.IEEE,2002.
5. E. Kalligeros, X.Kavousianos, D.Bakalis, D.Nikolos., “A New Reseeding Technique for LFSR-BASED Test Pattern Generation”.
6. Moriyasu, Takanori, and Satoshi Ohtake. “A method of LFSR seed generation for scan- based BIST using constrained ATPG”. Complex, Intelligent, and Software Intensive Systems (CISIS), 2013 Seventh International Conference on. IEEE,2013.
7. S. Nagaraju1, Ch.N.L.Sujatha2, J.S.S.Ramaraju3 “Test the S27 Benchmark Circuit by Using Built In Self Test and Test Pattern Generation”1M.Tech ECE Pursuing, Bhimavaram Institute of Engineering Technology, West Godavari, A.P, India Assistant Professor, Department of ECE, Bhimavaram Institute of Engineering Technology, West Godavari, A.P,India 3 Assistant Professor, Department of ECE, Bhimavaram Institute of Engineering Technology (BVRM), West Godavari, A.P,India.
8. Version Version 2 EE IIT, Kharagpur , “Testing of Embedded System”.
9. Version C. V. Krishna, A. Jalas, and N. A. Tauba, “Test vector encoding using partial LFSR reseeding”, in Proceeding of the International Test Conference, pp. 885-893,2001.
10. Mina Mishra, V.H. Mankar, “Text Encryption Algorithms based on Pseudo Random Number Generator”, International Journal of Computer Applications (0975 8887) Volume 111 No 2, February 2015.

AUTHORS PROFILE

Siripurapu Sridhar is currently working as a professor. He received doctorate in the year 2016. His research interests include generic Low Power and High Speed VLSI Neural Network architectures suitable targeting digital signal and image processing applications. He is currently working on VLSI Implementation and porting of neural network architectures relevant to significant applicable domain areas especially dealing with high speed multiplication algorithms. He is a life member of ISTE, Member of Institution of Engineers(India), Member of IEEE.

K.Mounika is presently pursuing B.Tech (ECE) Department of Electronics and communication engineering inLENDI INSTITUTE OF ENGINEERING AND TECHNOLOGY,Vizianagaram.

M.Anjali is presently pursuing B.Tech (ECE) Department of Electronics and communication engineering inLENDI INSTITUTE OF ENGINEERING AND TECHNOLOGY,Vizianagaram.

G.Venkatesh is presently pursuing B.Tech (ECE) Department of Electronics and communication engineering in LENDI INSTITUTE OF ENGINEERING AND TECHNOLOGY,Vizianagaram.

M.Murali Krishna is presently pursuing B.Tech (ECE) Department of Electronics and communication engineering in LENDI INSTITUTE OF ENGINEERING AND TECHNOLOGY,Vizianagaram.