International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9, Issue-7, May 2020

Low Power Bidirectional Voltage Level Translator using Power Gating

Smt. Y. Sujatha

Abstract: ***now a day's, the demand for SoC based systems increasing. In SoC environment, multiple supply voltages are required because various subsystems of the system operate with different supply voltages. The communication between these systems is difficult and increases power consumption. The solution to this problem is to use a Voltage level translator/shifter between them. In this paper, a low power voltage level translator using power gating is proposed. By using this translator bidirectional voltage translator is implemented. In bidirectional voltage level translator, the data is translation between core logic and pad drivers and vice versa is possible with reduced power consumption and delay. In this paper, the power consumption reduces from 104uw to 6.25 pw at Vdd 1.8V. Delay is reduced from 19ns to 0.2 ns.***

Keywords: Multiple Supply Domains, Pass Transistor Logic, Voltage Level Translator, Power Gating.

I. INTRODUCTION

A system on chip is an IC that integrates all the modules including core logic, memory and pad drivers etc. on a single chip. Generally core logic operates at low logic levels whereas input/output pad drivers operate at high logic levels. In order to communicate between these modules, it requires an interface called voltage level translator/shifter. A voltage translator/shifter translates the voltage levels from high to low or low to high. Instead of using multiple supply voltages, a voltage level translator saves power consumption.

To design systems with increased functionality, designers are facing lot of challenges because there is a requirement for low power consumption, high speed performance and time to market. Various subsystems of a system built with different process technologies. One system may be designed with one process technology works with high supply voltage (ex: *130nmCMOS at vdd=3.3v*) and the other system designed with another technology works with high supply voltage (TTL with vdd=5v). The selection of appropriate voltage translation device is determined by the process technology used for the circuit, power requirement, voltage translation levels and current sourcing capability of the device used.

A voltage Level translator is a circuit, translates a signals from one voltage domain to another.

Revised Manuscript Received on May 30, 2020.
***** Correspondence Author
Y.Sujatha*, ECE department, Sri Vasavi Engineering College, Tadepalligudem, INDIA. Email: sujatha1528@gmail.com

To translate from one domain to another, two different supply voltages are used. One supply voltage is used at the input. That means input is of that voltage level. Second supply voltage is used at the output. The output signal is at second supply voltage. Two inverters with cross coupling can be used to achieve full logic swing i.e. 0 to vdd at the output.

This paper is organized as five sections. In section I, a brief introduction to the voltage level translator is given. In section II, a brief explanation to the conventional voltage translator and its design is given. Section III, covers the design of proposed voltage level translator and bidirectional voltage level translator. Section IV, design of various applications using proposed design and a brief discussion on simulation results. Section V, discuss how the best the proposed voltage level translator like power consumption and delay.

II. CONVENTIONAL VOLTAGE LEVEL TRANSLATOR

This is the voltage level translator using two power supplies VDD1 and VDD2. VDD1 is used in the input section and VDD2 is used in the output section. This translator translates any signal from one voltage level VDD1 to another voltage level VDD2. Two NMOS transistors driver transistors receive input and complemented input. Two PMOS load transistors are cross coupled to obtain full output voltage swing.

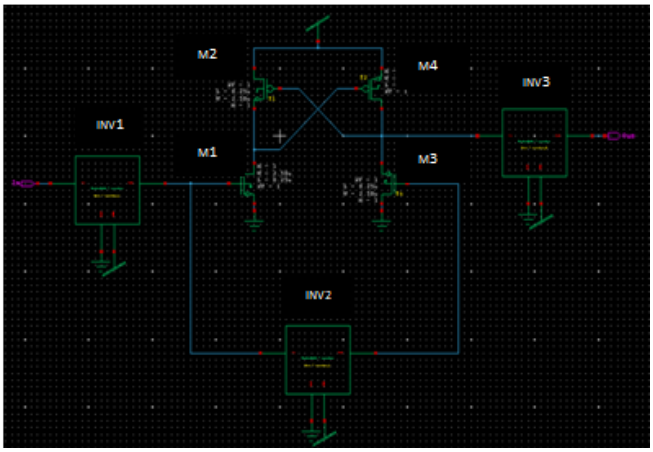


Fig.1: conventional voltage level translator

When VIN is high, the driver transistors M1and M3 receive '0' and '1' respectively. Then the transistor M3 is ON, and the output node_2 becomes low. This makes inverter3 output is high with VDD2 (high). So the voltage level translator translates the VIN at VDD1 (low) to VOUT at VDD2 (high) and vice versa. In this design, PMOS transistors are used as load. When the PMOS transistor is ON, it offers high on resistance. So, it takes more time to produce output.

Large delay is the main drawback with this circuit. So to overcome this drawback, the proposed voltage level translator is designed.

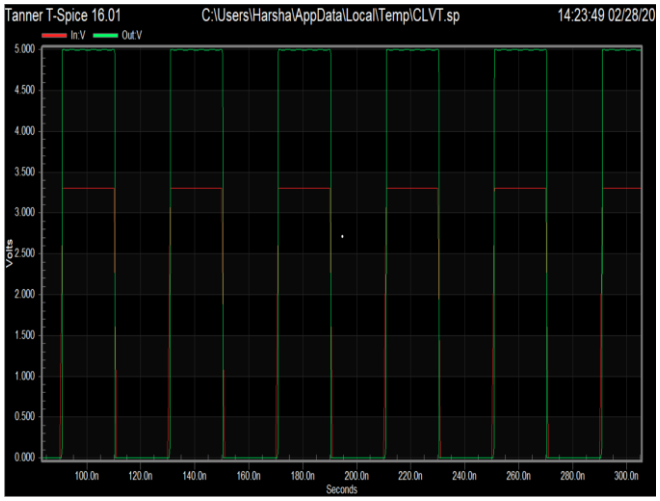


Fig.2: Output waveforms of the conventional voltage level translator

III. PROPOSED VOLTAGE LEVEL TRANSLATOR

In the proposed work, 1. Uni-directional voltage level translator 2. Bidirectional voltage level translator is designed

A. Unidirectional Voltage Level Translator

Fig.3 shows the unidirectional voltage level translator. This translator works based on three control signals EN, ENB, EN_MUX. For proper operation of the circuit, the enable inputs EN and EN_MUX must be low. VDD1 and VDD2 are the input and output supply voltages respectively. The transistors T1 and T10 are sleep transistors. When the enable input (EN) is low, the sleep transistors will turn ON, it performs its functionality. When EN is high, the sleep transistors will turn OFF, it eliminates the connection from the supply lines. It reduces power consumption when it is not functioning.

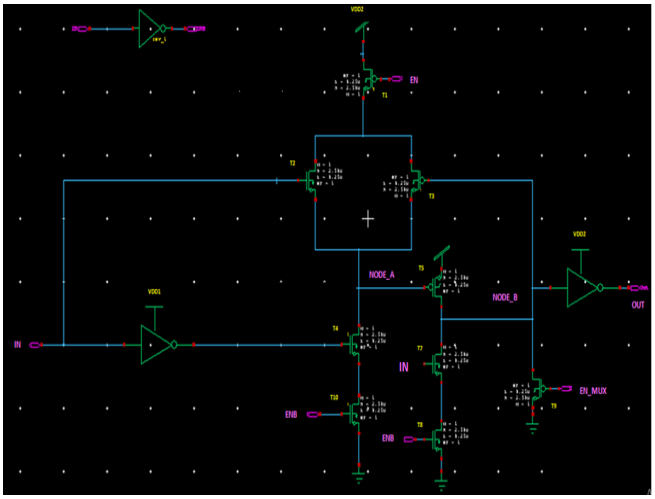


Fig.3: Proposed voltage level translator circuit.

In this design two inverters present. The inverter at the input operates with the supply voltage VDD1 and the inverter at the output operates with the supply voltage VDD2. Upon the circuit is enabled, if IN is low, the transistors T2 and T7 are turned off. The inverter at the input is operating with the low supply voltage VDD1. As the input to the inverter is LOW, output is equal to VDD1 (logic '1'). This turns ON the transistor T4 and the transistor T10 is already in ON condition. This pulls the node A low, which drives the transistor T5 ON. This pulls the node B high. Then the output of the output inverter becomes LOW.

Especially when the input is high, the transistors T7 and T8 are turned ON, which provides low resistance path to ground. This makes the output of the inverter is high with VDD2. Due to this path signal is propagated to output with very less delay.

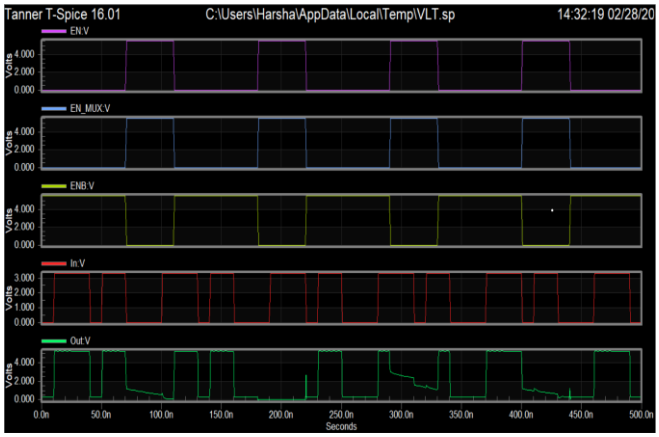


Fig.4: output waveforms of the proposed voltage level translator

B. Bidirectional Voltage Level Translator/shifter

Here the bidirectional voltage level translator/shifter is designed by using unidirectional voltage level translator. In SoC environment, generally core logic is operated at the low supply voltage and the pads operated with the high supply voltage. This bidirectional voltage level translator translates the data between these two and in both the directions. The following fig.5 shows the architecture of bidirectional voltage level translator.

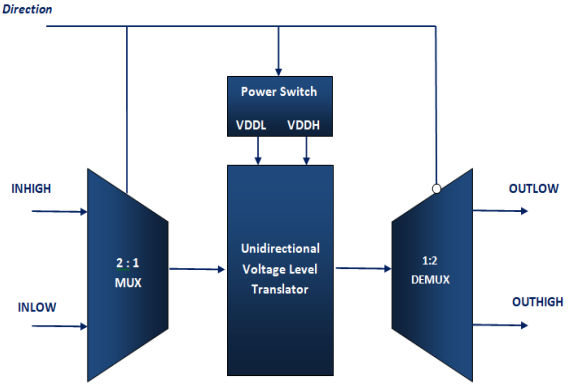


Fig.5: Bidirectional voltage level translator.

Here the direction signal is to select the direction of voltage translation: input/output pad to core i.e. high input voltage (INHIGH) to low output (OUTLOW) and core to input/output pads i.e low input voltage (INLOW) to high output (OUTHIGH). Fig.6 shows the design of bidirectional voltage level translator. When Direction=0, low input voltage is translated to high output voltage. When direction=1, high input voltage is translated to low output voltage.

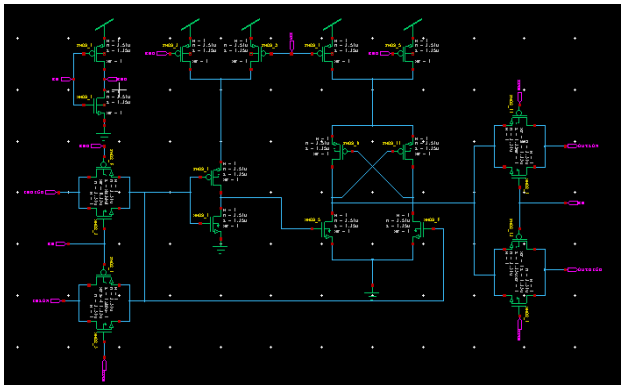


Fig.6 Design of bidirectional voltage level translator

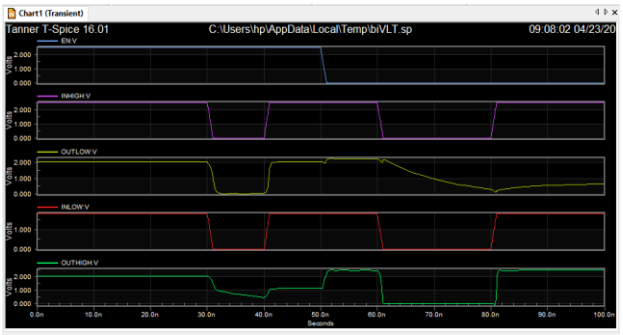


Fig.7 output waveforms of bidirectional voltage level translator

IV. APPLICATIONS

The proposed voltage level translator can be used to design the following applications:

a. Logic Multiplexer
b. Data storage in multi-supply design

A. Logic Multiplexer

Here two proposed voltage level translators are used to processutput supply voltages respectively.

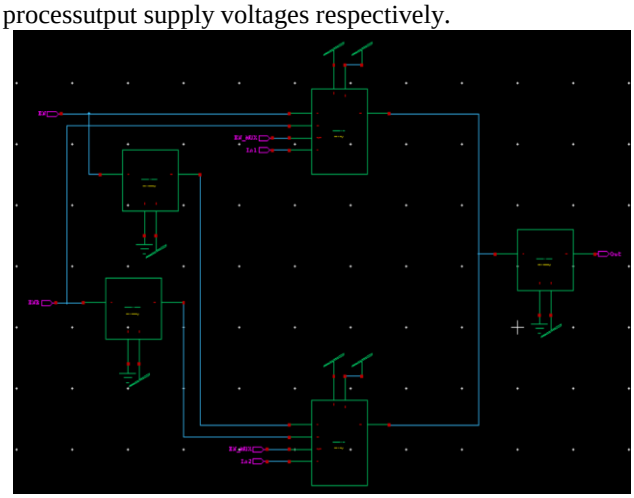


Fig.8: 2*1 multiplexer using voltage level translators

This multiplexer works based on the control signals EN,ENB, EN_MUX. IN1 and IN2 are the two inputs of the two proposed voltage level translators. For the correct functioning of the circuit the EN_MUX is always zero. When EN is logic 0 and ENB is logic1 then the output will be IN1. When EN IS logic1 and ENB is logic0, then output will be IN2. If we design this circuit with conventional voltage level translator, we get large delay and the power efficiency is very low.

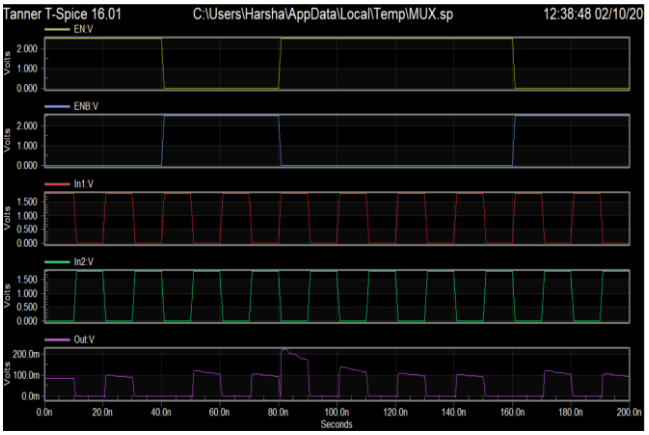


Fig.9: output waveforms of the logic multiplexer circuit

B. Data storage in Multi-supply design

In SoC, the output of various subsystems has to be stored in a memory device. In such cases, it requires a voltage translator between subsystems and memory.

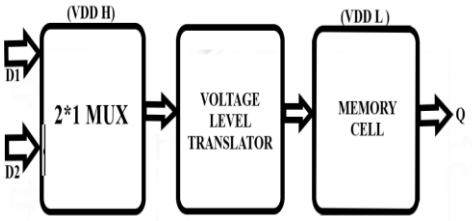


Fig.10: Circuit connection of the Multi-supply design

Design of 2*1 multiplexer

The 2X1 multiplexer selects the data from one of the subsystems based on the value of select line.

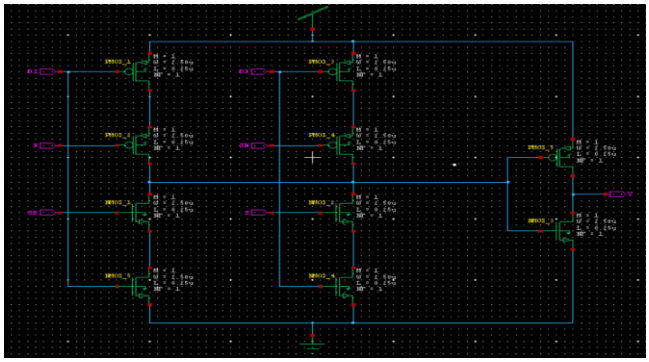


Fig.11: Circuit design of the multiplexer.

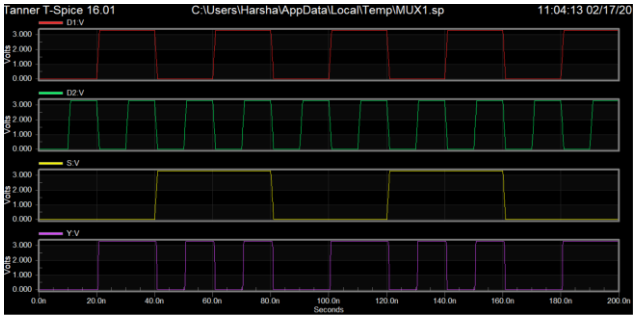


Fig.12: Output waveforms of the 2*1 multiplexer

Design of Memory cell

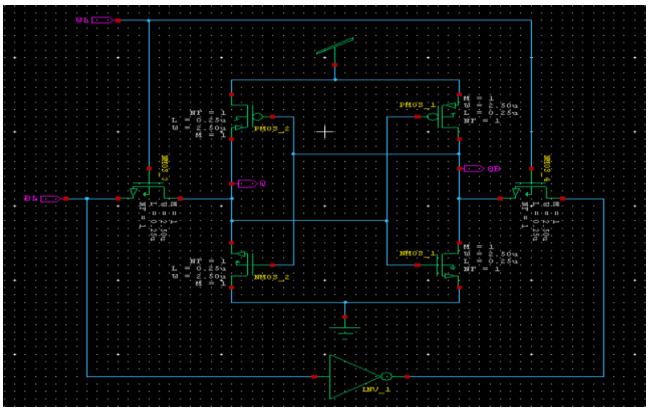


Fig.13: 6-transistor SRAM cell

Basic 6T SRAM can be used as a Memory cell. After voltage translation, the results are stored in the memory cell.

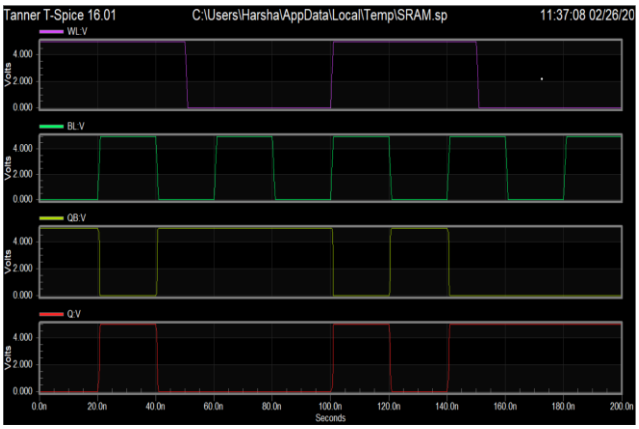


Fig.14: Output waveforms of 6T SRAM

Fig.15 shows the data stored in the memory cell in multi supply voltage environment.

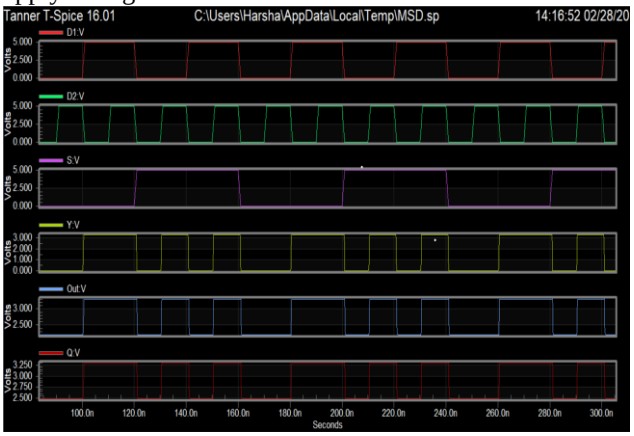


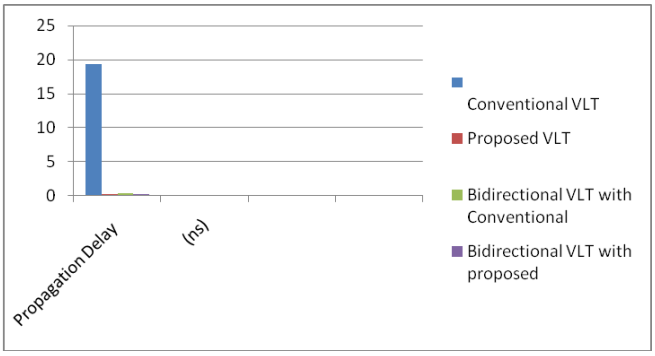
Fig.15: Output waveforms of the Multi-supply design

V. RESULT AND DISCUSSION

Low power unidirectional and bidirectional voltage level translators are designed. All the designs are simulated using TANNER EDA tools. The proposed voltage level translator consumes very less power 6.25pW compared to 104uW for conventional voltage level translator at the same supply voltage (1.8V). Table.1 shows the power consumption and delay at different supply voltages.

Table.1: performance comparison

Design	Power Consumption			Propagation Delay (ns)
	Vdd=2.5v	Vdd=1.8v	Vdd=0.9v	
Conventional VLT	2.501608e-004	1.048003e-004	1.175244e-004	19.29ns
Proposed VLT	1.089000e-011	6.250000e-012	3.240000e-012	0.2ns
Bidirectional VLT with Conventional	2.259000e-011	6.550000e-012	3.890000e-012	0.35ns
Bidirectional VLT with proposed	1.089000e-011	6.250000e-012	3.240000e-012	0.25ns



VI. CONCLUSION

A bidirectional low power voltage level translator is proposed in this paper. By using this bidirectional voltage level translator data translation in both the directions i.e. core logic (low voltage domain) to I/O pads (high voltage domain) is possible. Duo to the power gating technique, power consumption is reduced from 104uw for conventional voltage level translator to 6.25pw for proposed voltage level translator. And the delay is also reduced from 19ns to 0.2ns. So, it can be used for both high speed and low power applications.

REFERENCES

1. Syed Shakir Iqbal , "Low Power Robust Bidirectional CMOS Level Shifter" Emerging Trends in Electrical And Electronics Engineering (ETEEE-2015) Jamia Millia Islamia, New Delhi.
2. Dharshak B S and Rahul M. Rao, "A High Performance Gated Voltage Level Translator with Integrated Multiplexer," 31th International Conference on VLSI Design and 2018 17th International Conference on Embedded Systems, 2018, pp. 358-361
3. Volkan Kursun and Eby G. Friedman, "Multi-voltage CMOS Circuit Design", ISBN:978-0-470-01023-5, Wiley Publications
4. Marco Lanuzza, Pasquale Corsonello and Stefania Perri, "Low Power Level Shifter for Multi-Supply Voltage Designs", IEEE Transactions on Circuits and Systems II: Express Briefs, DOI:10.1109/TCSII.2012.2231037, Volume:59, Issue:12, Page(s): 922-926, December-2012
5. Sherif A. Tawfik and Volkan Kursun, "Low Power and High Speed Multi Threshold Voltage Interface Circuits", IEEE Transactions on Very Large Scale Integration Systems, DOI: 10.1109/TVLSI.2008.2006793, Volume: 17, Issue:5, Page(s):638-645, April-2009
6. Stuary N. Wooters, Benton H. Calhoun and Travis N. Blalock, "An Energy-Efficient Sub-threshold Level Converter in 130nm CMOS", IEEE Transactions on Circuits and Systems II: Express Briefs, DOI:10.1109/TCSII.2010.2043471, vol:57, no:4, Page(s):290-294, April-2010
7. Wenfeng Zhao, et al, "A 65nm 25.1ns 30.7fJ Robust Sub-threshold Level Shifter with Wide conversion Range", IEEE Transactions on Circuits and Systems II: Express Briefs, DOI:10.1109/TCSII.2015.2406354, Volume: 62, Issue:7, Page(s):671-675, July-2015

8. Marco Lanuzza, Pasquale Corsonello and Stefania Perri, "Fast and Wide Range Voltage Conversion in Multi supply Voltage Designs", IEEE Transactions on Very Large Scale Integration Systems, DOI:10.1109/TVLSI.2014.2308400, vol:23, no:2, p:388-391, Feb-2015

AUTHORS PROFILE

Sujatha Y, completed Bachelor of Technology in ECE from JNTU Kakinada in 2003 and M.Tech (VLSI System Design) from JNTUH. Currently, working as Sr. Asst. Professor in Sri Vasavi Engineering College, Tadepalligudem and have 17 years of teaching experience. Her area of interest is Low Power VLSI Design.