

Enhancement of Short Channel Effect and Drain Induced Barrier Lowering in Fin-FET

Jagtap Sarika Madhukar, Gond Vitthal Janardan



Abstract: The essential requirement of any battery-operated and mobile devices like laptops, cellular phones are that they must be small in size, consume less power, fast processing and cheaper expansion. Gordon Moore found in 1965 that the quantity of transistors on a chip will drive to be twofold every year, by manufacturing the portable devices and building circuit on the silicon chip which makes device cost effective. This drop in size of transistor is termed as scaling. Since scaling faces formidable challenges in nanometer regime, successors have been emerged as FinFET's. They have thin fin or wing like channels enclosed by several gates. Due to many gates the design helps to improve performance and boost energy efficacy. Present work highlights the role of scaling and how scaling improves the speed of the device. The expectation from the scaled device is to consume as low power as possible, effective in costs and less design time. As we make the instrument more portable, complexity in it becomes infinite. Moore's law supports us to realize the role of scaling to improve circuit performance and make a portable/mobile device. Here, we design 14nm, 10nm and 7nm Triple gate Fin-FET (TG Fin-FET) and investigate the Drain Induced Barrier Lowering (DIBL) and Short Channel Effect (SCE). By scaling the device DIBL and SCE are reduced giving better performance in terms of power and speed.

Keyword: BSIM, Fin-FET, Modeling, MosFET.

I. INTRODUCTION

Electronic trade markets are presently directing on shrinking the dimensions of devices and are into carrying products in compact sizes with higher speeds and power efficiencies. Scaling has been expected towards smaller size, developed speed, lower power and thickness of the semiconductor devices. As MOSFET scale the gate length into nanometer region, the switch or control over the channel from the gate terminal declines and uninvited dilemma such as hot carrier effect and short channel effects take place. Technology node has shrunk from 10 micrometer in 1971 to 45 nanometer in 2004 and will shrink to below 10 nanometer in 2018. As we condense the magnitude of the transistor, further undesirable cross effect come into picture, and this effect is called as the short channel effect. In short channel device, the length L of the channel varies from μm to nm reducing the distance between source and drain.

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Therefore, we always consider the proximity(nearby) effect, whereas in long channel MOSFET, this scope is of considerable length. As the channel dimensions are shrinking, it takes the advantages of area utilization, various effects such as rise in source-drain leakage current, significant variations in device performance due to uncontrollable channel doping.

Enhancement of SCE in short channel MOSFET like threshold voltage roll-off, DIBL, Punch through, leakage current, mobility degradation arises due to scaling. FETs act as active devices in the bulk planar transistor technology, while Fin-FETs has silicon on insulator (SOI) and bulk quasi-planar transistor technology. Fin FET's have better electrostatic supervisor of multiple gates to set conventional full semiconductor channel, which decreases the short channel effects.

II. FIN-FET DEVICE:

The MOSFET is planar device and having channel parallel to substrate, whereas in Fin-FET device the channel is thin and wraps perpendicular to substrate, i.e. the gate is fully "covered" around the junction formed between the source and drain. The current travels are conforming to the level while the conducting channel is shaped near the Fin edges. The gate works fast to fully exhaust the conducting path, thus intensifying the electrostatic control over the channel.

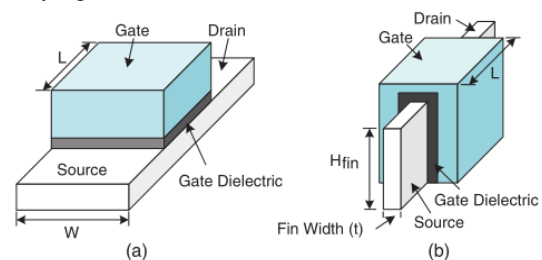


Figure 1: Device Structure (a) MOSFET Device (b) Fin-FET Device.

Fin-FETs is mainly of dual type structure generally identified from its gate terminal as,

1. Shorted-gate (SG) Fin-FETs
2. Independent- gate (IG) Fin-FETs.

In Shorted Gate devices, both the gates are connected and composed in a wrap-around structure as seen in Figure 1(b), which can be directly related to the planar devices having gate, source and drain as seen in Figure 1(a). In Insulated Gate Fin-FETs, the top portion covering around the gate structure shows the thickness of fin, whereas, front and back sides of gate make the design as triple gate Fin-FET with single source & drain terminals which can be controlled separately.

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Depending on the substrate, the Fin-FETs can be either SOI or bulk quasi planar.

This paper elaborates and makes an attempt to clarify the scaling used to improve the device performance, helps to understand long channel and short channel effects on devices, along with the construction details of MOSFET and Fin FET's. We observe the effects of geometrical parameters like gate length, Fin height, Fin thickness variations on the performance of TG Fin-FET. After designing Single Fin-FET with triple gate device successfully, we present their current and voltage [I - V] characteristics and transfer characteristics. By the support of these characteristics' features and by using high doping concentration with Fin thickness and gate length variations, the value of SCE and DIBL are measured. The choice of Fin thickness, gate length and doping concentration varies as per the designing of the device.

Physical Parameters used in the Design of Single Fin-FET:

Table 1 Geometry Parameters used in Fin-FET Design:

Sr. No	Device Parameter	Symbol	Value [N-Fin-FET]
01	Height of Fin	H_{Fin}	90[nm]
02	Width of Fin	W_{Fin}	100[nm]
03	Fin Thickness [Depth]	L_{Fin}	30 and 10[nm]
04	Gate Length	L_G	30[nm]
05	Gate Height	H_{gate}	60[nm]
06	Gate Work Function	ϕ_g	4.1
07	Oxide Thickness	T_{ox}	1[nm]
08	Drain Voltage	V_d	10mv
09	Gate Voltage	V_g	1V
10	Gate Material	Si	Si
11	Oxide Relative Permittivity	ϵ_{ins}	6.9
12	Channel Doping Concentration	N_{A0}	$1e19[1/cm^3]$
13	Source/ Drain Doping concentration for NMOS	N_{D0}	$1e21[1/cm^3]$
14	Junction Depth	d_j	1[nm]

III. DEVICE STRUCTURE

The different geometry parameters considered for structure of device design in this paper are stated in Table 1. The Fin-FET construction is created on a vertical silicon Fin characterized by the gate length (L_G), Fin height (H_{Fin}), and the silicon thickness (T_{Fin}).

3.1 Introduction to Short Channel and Long channel device

We need Fin-FET or Tri-Gate or Fully Deflected-SOI kind of devices to reduce short channel effects and need to move from planar to non-planar architecture. Here in Figure 2 conventional transistor structure having source, drain and channel are shown where the channel is formed for both Long and short channel devices.

When we apply voltage to gate terminal by gate field, electrons flow from source to drain. We see an exponential increase in I_{DS} as a function of V_{GS} . Two things to point out here is essentially the slope of this exponential increase which is known as the subthreshold slope (SS), and another thing to point out is the voltage at which we start seeing this exponential increase in I_D i.e. the threshold voltage (V_{TH}), as observed in Graph 1.

The V_{GS} versus I_{DS} i.e. transfer characteristics of MOSFET are shown in graph 1. From the curve, we perceive that in the sub-threshold region ($V_{GS} < V_{TH}$) the value of total drain

current depends on exponential value of V_{GS} , and can measure threshold voltage at that respective point.

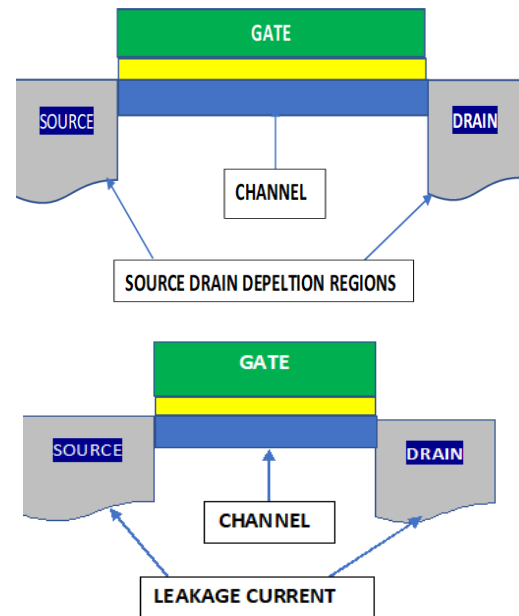
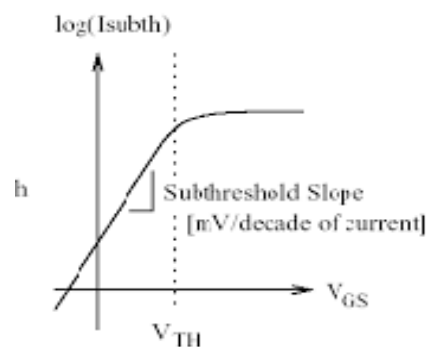
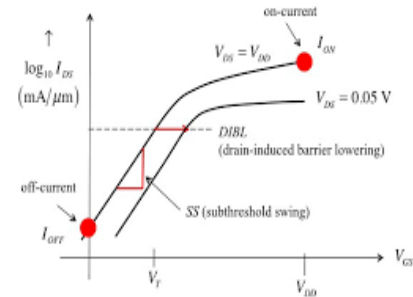


Figure 2: Conventional transistor showing long and short channels



Graph 1: I-V characteristics

In the stretched (long) channel transistor, when the V_{GS} ranges from a low value (0.05V) to a more considerable amount (1V), increase in on state drain current as well as a similar increase in off state drain current is observed. The subthreshold slope also increases lowest to highest.

In short channel device, gate length is scaled below 22nm in accordant with 14nm, 10nm and 7nm. At lower drain voltage, the device behaves like MOSFET,

where an exponential increase in I_D is observed at start of V_{TH} . While, at higher values excessive energy tends to affect potential barrier which exists for electrons to flow from source and drain, and we see the lowering of the fence due to inducing of drain voltage.

This induced drain lowers the barrier hence known as DIBL. So, three things are been observed in short channel devices

- increase in drain voltage degrades the subthreshold slope,
- reduction in threshold voltage V_{TH}
- escalation in off-state current.

These three belongings usually are known as SCE. All these SCE are unhealthy for device performance. So, we have to reflect on new physical MOS structure performing equally well.

International Technology Roadmap for Semiconductor studies the Fin-FET as a required applicant to switch the planar MOSFET to non-planar technology in the multi-gate device structure. The geometry used for the designing Single Fin-FET and Multi -Fin-FET is discussed here. Also, by varying Fin thickness and gate length the effect on SCE and DIBL is measured.

IV. FIN-FET TECHNOLOGY:

A switch is the heart of CPU's processing power. The CPU consists of large number of transistors, which act like switch, that performs numerous tasks. The function of switch is to either block or pass the current in the respective network. Depending on how fast the transistor switches, the consumption of power is decided. In the ordinary transistor, we place three-electrode Source, Drain and Gate. Source and drain passes the current into the channel, which forms a path; this is one type of switch which is on which gives the flow from source to drain and middle portion works as a channel. To switch off the channel, we apply the potential which closes the circuit with the help of PN junction. By applying more voltage, the channel is going to close and current start flowing from source to drain this in planar technology. For better performance of the processor, large transistors are used, so the size of transistor needs to shrink more and more and 14nm is the size of transistor we have small portable and to connect them in series or in parallel making network for CPU designing. Once we shrink the device, source and drain show proximity between them gate losses the control over the channel. To solve this problem, INTEL introduces Fin-FET. In processor, by using Fin-FET technology multiple gates, so processing power is more and rapidly it processes the data so need to increase of transistor. Means that in an off state also, still some current flows through the source to drain. To solve this issue, we make a metal contact on top side there is a gate, now we place gate 3D on three sides from all side control over the gate increases as we put the gates on three sides. Gate never controls the channel from one side it controls from all side while in planar transistor it controls from the only top side. As we place gate from three side gate control over the channel is increases as we place potential across gate the current from source and drain block.

As in planar transistor gate controls the channel from the top, it doesn't deplete from the other two sides, so the channel is not entirely off. So, in normal condition leakage current flow

and 3Dimensional by placing gates, it controls the current and very low leakage current flow in the device. Thus, power loss in this situation is minimized, so processing power increases. As the device shrunk, the performance increases gate control increases leakage current decreases and processor use less energy.

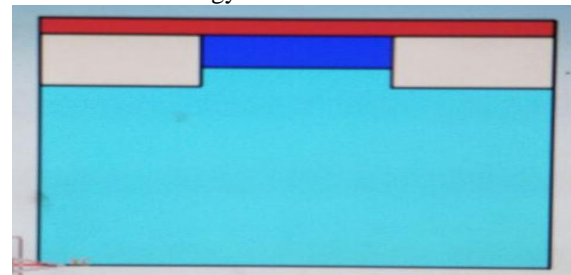


Figure 3: Top view of MOSFET

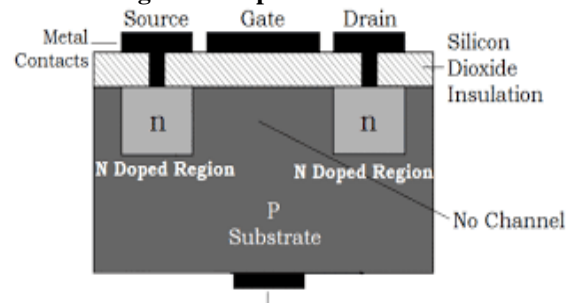


Figure 4: Construction of MOSFET

Figure 3 & 4 shows construction of MOSFET represents single gate with source & drain terminals a lightly doped substrate, is diffused with a heavily doped region.

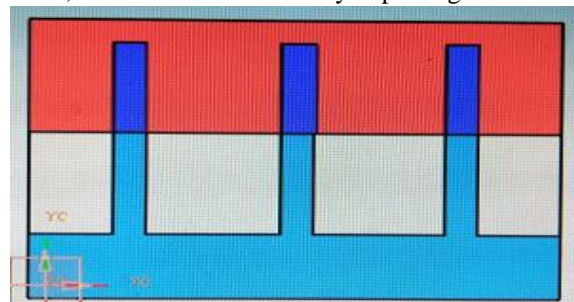


Figure 5: Front View of Fin-FET Structure

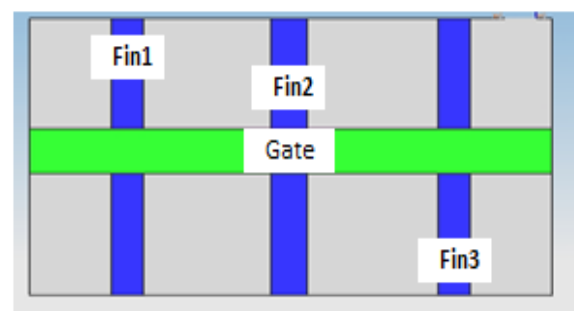


Figure 6: Fin-FET Structure

In a planar device like MOSFET, the source and drain are self-aligned with the gate whereas in Quasi Planar Fin-FET device there is a nitride spacer between the gate and the source and drain, which are usually raised. After technical progress on the dual-gate MOSFET building, a most excellent construction obtained using a Fins between two end-to-end gates, called Fin-FET.

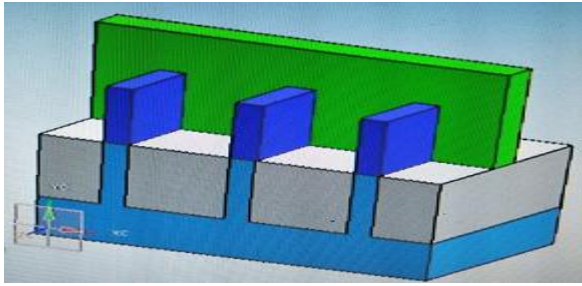


Figure 7: Multi Finger Fin-FET

Contribution of top gate grades the tri-gate and top gate oxide width chooses the energy of high gate. Fin-FET is a multi-gate creation in which Si film forms the channel and gate covers around the Fin. A natural insulator layer placed lower the top gate and sidewalls of Fin. The current travels are corresponding to the device sides [15]. Serious problems created in the conventional planar MOSFET structure below 45nm scaling like increase leakage current, SCEs, threshold voltage variations which are improved by Bulk Fin-FETs and SOI Fin-FETs structures [16].

V. FIN-FET TECHNOLOGICAL DESIGN PARAMETERS

The channel width W of Fin-FET transistor is in terms of Fin height (H_{Fin}) and Fin width (W_{Fin}).

$$Fin\ Width = 2HF_{in} + WF_{in}\#(1)$$

The required current of the device can obtain by several Fins n_{Fin} corresponding structure (width quantization), and effective channel width will be $n_{Fin} \times Width$.

Fin height should be smaller than fin width, which gives the more suppleness to the design and leads to many Fin design concept, so more area is essential on the silicon chip. Taller Fins provide the ambiguity and less part to the proposal. As per the design rule, it must be below four times the Fin width [16]. The gate length (L_G) oxide thickness (t_{ox}), Fin width (W_{Fin}), Fin height (H_{Fin}), Spacer, Fin shape (circular, rectangle) corner radius are physical.

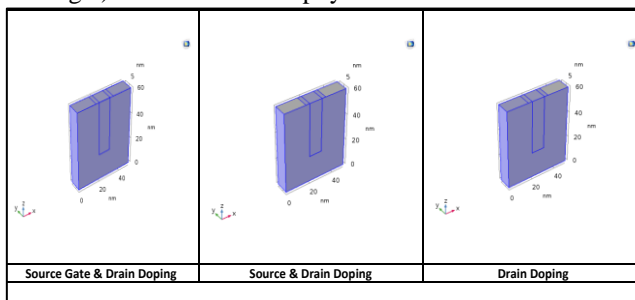


Figure 8: Geometry of 3D Fin-FET

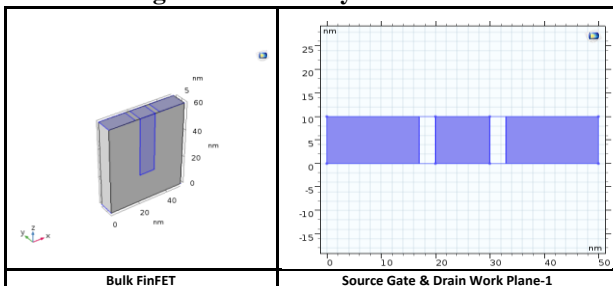


Figure 9: Structure of Fin-FET

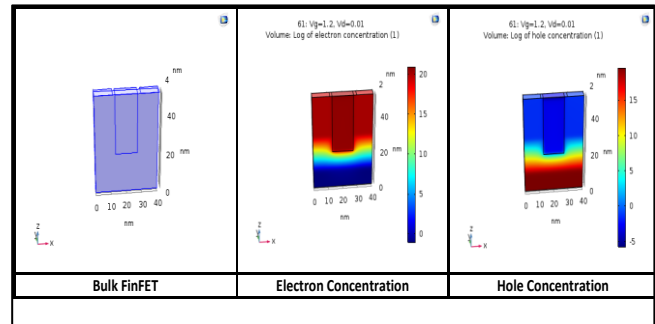
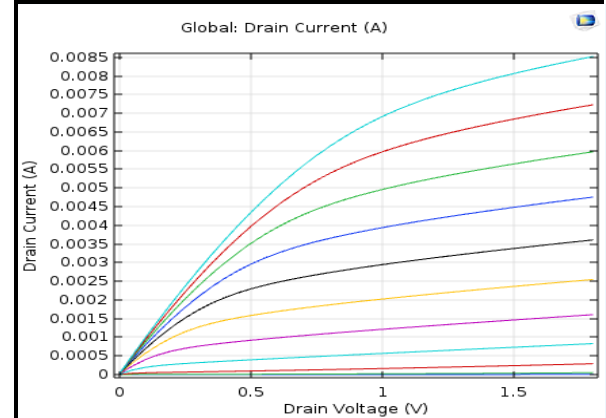
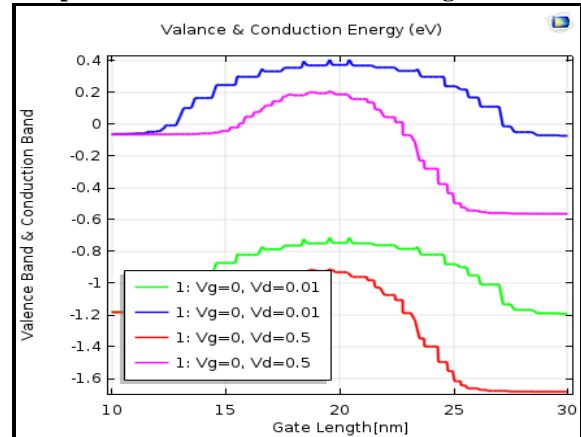


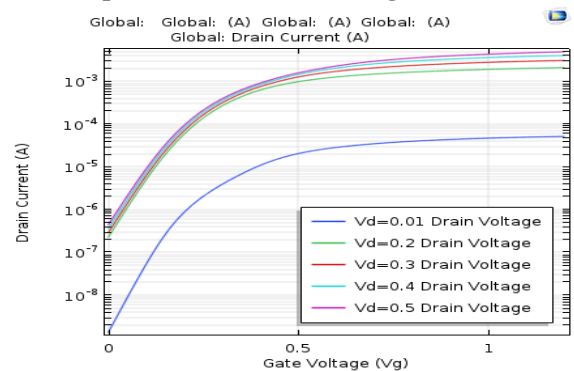
Figure 10: Fin-FET Electron & Hole Concentration



Graph 2 I-V Characteristics 7nm Single Fin-FET



Graph 3 DIBL Curve for Single Fin-FET



Graph 4 Transfer Characteristics of Fin-FET

5.1 Short Channel Effects on MOSFET

As the size of the MOS devices summarized, there is a closeness between the source and drain, which declines the capacity of the gate electrode to switch the possible spreading.

The movement of leakage current in the channel region and undesirable result arises that conclusion is called Short Channel Effect.

A most crucial cause of SCE is the bead in the threshold voltage with weakening channel length. Threshold voltage decrease causes the off current (Leakage Current) of a MOS transistor to surge significantly, thus giving growth to advanced static power dissipation. Following are dominants SCE occurs in MOSFET:

1. Drain Induced Barrier Lowering
2. Subthreshold Leakage
3. Punch Through
4. Velocity Saturation
5. Mobility Degradation
6. Channel Length Modulation

DIBL is basically the outcome of channel energy on output transmission and measure the device conduction voltage i.e. threshold voltage. This spectacle / phenomenon is occurring where one / solitary gate terminal length is cuts lacking any other extents. It finds that difference in the threshold voltage with reduced gate length. It can be removed by proper scaling of source and drain depth and increasing substrate doping density. SS shows how fast MOS transistor turns off when V_{GS} reduced below the threshold voltage. A low value of subthreshold is desirable, and it can attain by using a thinner oxide layer or lower body doping.

As device size is compact, the power-driven fields also growths and velocity of carriers in the channel rises. So, showing the device at minimal dimensions is a very critical task. Fin-FET has minor gate leakage, more reliable gate control, reduced SCE, and less performance variability compared to bulk CMOS. The device is called as Fin-FET because the silicon looks like the dorsal Fin of a fish.

5.2 Short Channel Effect significance:

As we scale the size of the transistor, in this case, undesirable side effects occur called a short channel effect. SCE occurs when the channel length is the same order of magnitude as the depletion layer width of the source and drain junction.

$$SCE = 0.22 \left(\frac{e_{si}}{e_{ox}} \right) \left(1 + \frac{x_j^2}{L^2} \right) \left(\frac{t_{ox} t_{dep}}{L} \right) V_{bi} \#(2)$$

e_{si} is permittivity of Silicon

e_{ox} is permittivity of gate oxide

X_j is source and drain junction depth

L is effective channel length

t_{ox} is gate oxide thickness

t_{dep} is the penetration depth of the gate field in the channel region

V_{bi} is the source and drains built-in potential

SCE can be minimized by multiple gates and dropping the junction depth and gate oxide thickness. With the help of metal work function, dielectrics material, by changing Fin thickness, we can minimize SCE.

5.3 Drain Induced Barrier Lowering Significance:

As the device shrinks the influence of the subthreshold swing increases. When the channel length is sufficiently large, the source and drain junctions will be apart from each other such that they will not affect each other. By decreasing the channel length under a certain limit, the space charge at the drain will interact with that at the source leading to the potential barrier lowering at the source to the channel.

$$DIBL = 0.26 \left(\frac{e_{si}}{e_{ox}} \right) \left(1 + \frac{x_j^2}{L^2} \right) \left(\frac{t_{ox} t_{dep}}{L} \right) V_{ds} \#(3)$$

e_{si} is permittivity of Silicon,

e_{ox} is permittivity of gate oxide

X_j is source and drain junction depth

L is effective channel length

t_{ox} is gate oxide thickness

t_{dep} is the penetration depth of the gate field in the channel region.

V_{ds} is a drain-source voltage.

In the present work, we design Single Fin-FET with 14nm gate length and observe SCE, DIBL by changing Fin thickness from 7nm, 10nm, 14nm.

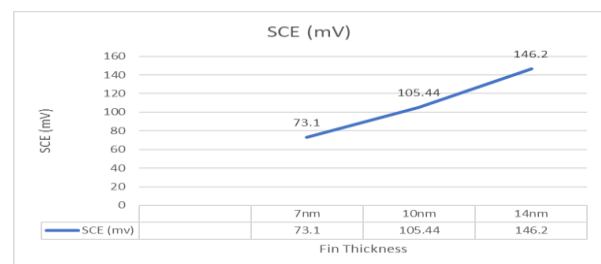
VI. RESULTS AND DISCUSSION

Fins of Fin-FET plays very crucial role when the device is operated. If Fin thickness is narrowed, it leads to quantum confinement. This confinement rises the threshold voltage by reducing density of minority carriers lowering down the leakage current. On the other hand, widening the Fin, rises the leakage current as the control of gate terminal is vanished. DIBL is highly dependent on variation on fin width on. Smaller the fin width has the good control over the DIBL. As the gate length of the device scale, the gate has ability to control the distribution of voltage & current control by sharing SCE & DIBL SCE & DIBL can be reduced by reducing junction depth, gate oxide thickness.

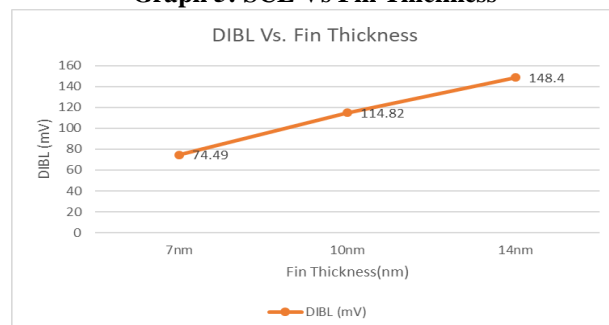
Designing the devices with said specifications, gives the results noted in Table 1. These results are graphically plotted in Graph 5 and Graph 6 respectively.

Table 2: Result on SCE & DIBL by varying Fin thickness

Gate Length	Fin Thickness	SCE (mV)	DIBL (mV)
14nm	7nm	73.1	74.49
14nm	10nm	105.44	114.82
14nm	14nm	146.2	148.4



Graph 5: SCE Vs Fin Thickness



Graph 6 : DIBL Vs. Fin Thickness

The result demonstrates better performance of scaled device i.e. as the fin width reduces from 14nm to 7nm, the values of SCE and DIBL are lowered to great extent.

VII. CONCLUSION

Device design of Fin-FET with different geometry parameters is the way to understand the functioning of the device. The work provides by using geometry parameters like fin height, width, doping concentration we design the device and investigates the two effects as the short channel effects and the drain induced barrier lowering. Short Channel Effect can be minimized by reducing Fin thickness and gate oxide thickness. Different geometry parameters use for the design of the triple gate, and Single Fin-FET devices are design and its effects observed on SCE and DIBL. By decreasing T_{ox} , the plan can provide better channel control. Doping concentration is a crucial design parameter in the measurement of SCE. It should be kept as low as possible. Observation of DIBL effect in different nm regions for Multi-Gate device. This work gives an insight knowledge of the effect of scaling, construction of MOSFET, need of Fin-FET and its salient features of Fin-FET. 3D simulation and geometry parameter variations of Fin-FET designs presented. Fin-FET designs for 14nm gate length and different Fin thickness for (14nm, 10nm and 7nm) for single Fin-FET. For long channel effect, pinch off occurs at overdrive voltage ($V_{gs}-V_t$). For short channel effect, pinch off occurs at lower values of overdrive voltage.

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