

# Smart Traffic Controller Implementation using FPGA



Sowmya KB, Sagar T, N R Pavan Santosh

**Abstract:** Every second heart attack patient in India takes 7 hours to reach a hospital, which is almost 14 times more than the ideal time within which a heart patient should be treated that is 30 minutes, government data shows. A two-year data from the ongoing Management of Acute Coronary Event (MACE) Registry of the Indian Council of Medical Research (ICMR) shows at some places it even takes 15 hours. A lot of precious time is still being wasted in traffic. Also some lines in the traffic junction are prone to traffic than the other lines and all the lines are held green for the same time irrespective of the density of traffic. The FPGA (Basys-3) based traffic controller sets the light green of a line if it detects ambulance (using sound sensor) in that particular line. Also if the density (determined using IR sensor) in one of the lines is high that particular line is held green for longer time.

**Keywords:** Traffic light controller, FPGA, sound sensor, IR sensor

## I. INTRODUCTION

The FPGA based controller is designed as a time-based traffic light control system for a junction having four ways. There is an internal decremented counter which is used to display the signal time in a decremented order and also to change the signal from on path to another sequentially. Ambulance is given the highest priority. Sound sensors are placed on each of the four paths. The sensors are configured to trigger at ambulance frequency (900-1000 Hz). If the sound sensor triggers this path is made green and the ambulance is allowed to pass.

Next level of priority is given for the road density at any moment, especially during peak hours of going to or from work and schooling the traffic stays at its peak and regular waiting intervals are of no good use in these situations. Hence from the continuously monitored data for density when a certain road experiences the waiting time needs to be increased between 2 successive (orthogonal) roads, in this implementation there are IR sensors placed at both the bank of the road at the dotted lined markings (as shown in figure 1), hence whenever vehicles surpass that dotted line for a prolonged time (this ensures that it is traffic and not every vehicle that passes between that sensor continuously throughout the day)

the green light time is increased to accommodate all the traffic. We need to increase the delay for the light accordingly for all the roads whenever this situation occurs such that all the vehicles stranded in that road are cleared and only then moved to check the other roads. The last priority is given to the regular condition when there is neither ambulance nor higher traffic, all four roads are successively let to clear by turning then GREEN and others into RED (but the one right after being YELLOW instead) and this continues into all four paths until any higher priority condition is detected.

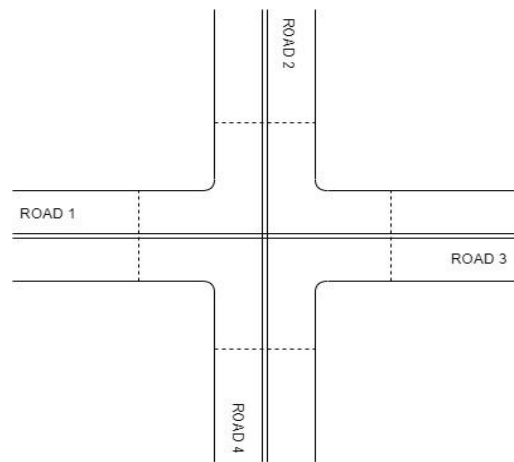


Fig.1. Traffic layout (dotted line indicate sensor positioning)

The following flow chart illustrates the functioning of traffic controller:

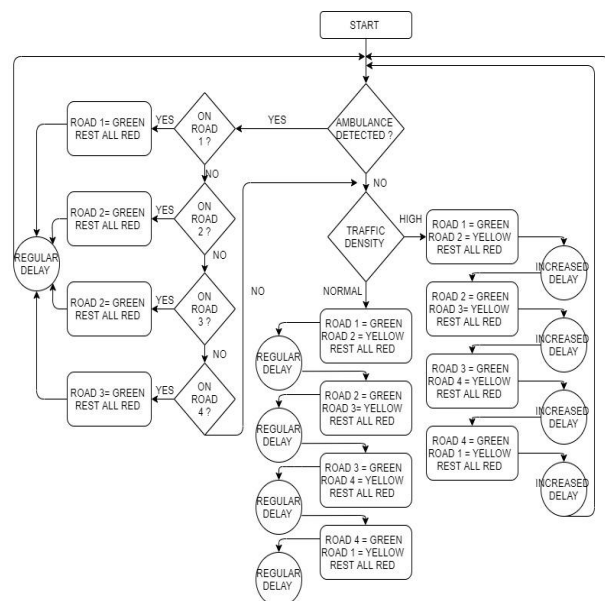


Fig.2. Finite state machine of the Smart Traffic Controller

Revised Manuscript Received on June 30, 2020.

\* Correspondence Author

**Sowmya K B\***, Assistant Professor, Department of Electronics and Communication Engineering, PA College of Engineering, Mangaluru, India.

**Sagar T**, Department of Electronics and Communication Engineering, PA College of Engineering, Mangaluru, India.

**N. R Pavan Santosh**, Department of Electronics and Communication Engineering, PA College of Engineering, Mangaluru, India.

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open access article under the CC BY-NC-ND license (<http://creativecommons.org/licenses/by-nc-nd/4.0/>)

## II. CASE ILLUSTRATION

### A. Case 1

Normal condition when there is no other higher priority signal detected (ambulance or density). The roads are provided with 8 cycles (80ns) GREEN, 4 cycle (40ns) of YELLOW followed by RED until all other roads also complete their GREEN and YELLOW condition. It runs in a successive manner as ROAD 1, 2, 3 and 4, and hence repeat this cycle until any signal detected.

### B. Case 2

This shows the condition when an AMBULANCE is detected anytime. The road on which the sound signal is caught is given the highest priority then and no matter what state it was in it switches to GREEN to allow the AMBULANCE to pass by.

### C. Case 3

This is to display the case when an AMBULANCE is detected any number of time, whenever the priority is asserted the system turns that certain road into GREEN to allow the emergency situation to be handled accordingly.

### D. Case 4

This shows the case when density is detected. Density on relative to the state the road is on when the signal is received, if we detect high density on a road that is being let out i.e is in GREEN already only then we increase the time of that state to allow all the vehicles to be cleared off. Here in the test condition ROAD 1 detects high density for a minimum of 8 cycles, because if the density signal is anywhere less than the available GREEN time it means that the vehicles could have been let out easily. Since we are measuring the density by placing sensors across the sides of the road after a certain distance from the intersection it ensures that any random vehicle passing through it doesn't trigger the signal so only when it stays on for minimum of 8 cycles (regular time) it shows the presence of excessive vehicles. When the required criteria are met the road is given more GREEN time than the regular interval which is  $8 + 16$  (excess time) = 24 cycles to ensure that the traffic is fully cleared off from that particular road.

### E. Case 5

This shows the probable condition when density is detected in a road that is currently not on GREEN, the density is ignored and the usual state is carried on. The pertaining problem with a response to a road that is not on GREEN is that if we increase the time interval for the road with density other roads have to wait for longer interval in their current condition (if some road has less vehicle but still has to be on green longer than required hence wasting time). Now a probable solution might be to give priority to that road even when it's not on GREEN and instead turn it into GREEN, but by doing this we are increasing the traffic on all other remaining roads and disturbing the smooth flow of traffic.

### F. Case 6

This shows the probable condition when density is detected in a road that is currently not on GREEN, the density is ignored and the usual state is carried on. The pertaining problem with a response to a road that is not on GREEN is

that if we increase the time interval for the road with density other roads have to wait for longer interval in their current condition (if some road has less vehicle but still has to be on green longer than required hence wasting time). Now a probable solution might be to give priority to that road even when it's not on GREEN and instead turn it into GREEN, but by doing this we are increasing the traffic on all other remaining roads and disturbing the smooth flow of traffic.

### G. Case 7

This shows the total working of the system, it works normally as intended in the circular manner as ROAD 1, 2, 3 and 4 successively until any priority signal. Given there is a density detected on a road which is currently at GREEN then the response is given such that it's GREEN time is increased such that the road clears out, and anytime in between if an AMBULANCE (being our highest priority) is detected that road is turned into GREEN to respond to the emergency.

## III. SCHEMATIC AND FPGA IMPLEMENTATION

GPIO pins can be used to interface the sound and IR sensor with FPGA. Output digital pins can be control to relay which will drive the traffic light (red, green, yellow). The internal clock of Basys-3 (100Mhz) is used as counter for lights.

The following is a schematic of FPGA implementation:

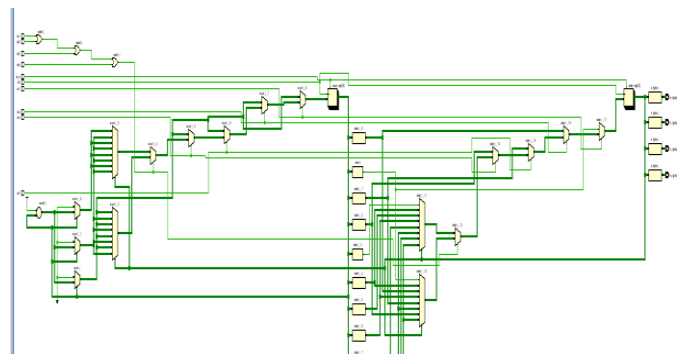


Fig.3. RTL Schematic of Smart Traffic Controller

## IV. RESULT ANALYSIS

Simulation waveforms for all the cases is shown in Fig.3, Fig.4, Fig.5, Fig.6, Fig.7, Fig.8 and Fig.9.

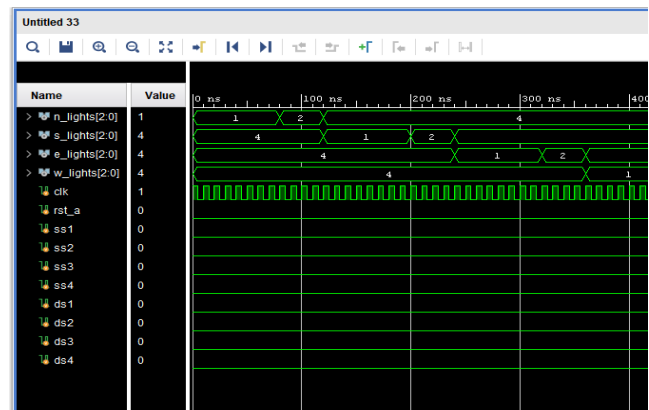


Fig.3. Case 1 simulation results

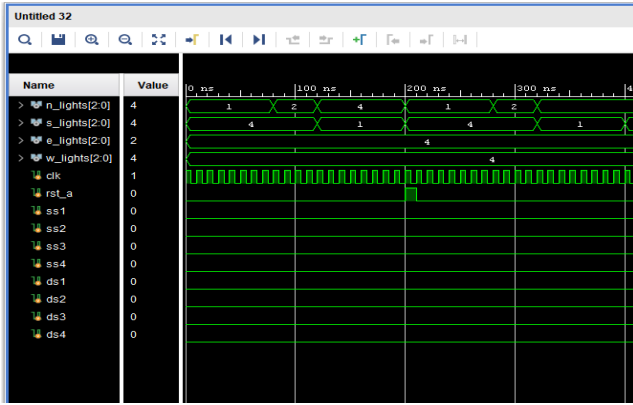


Fig.4. Case 2 simulation results

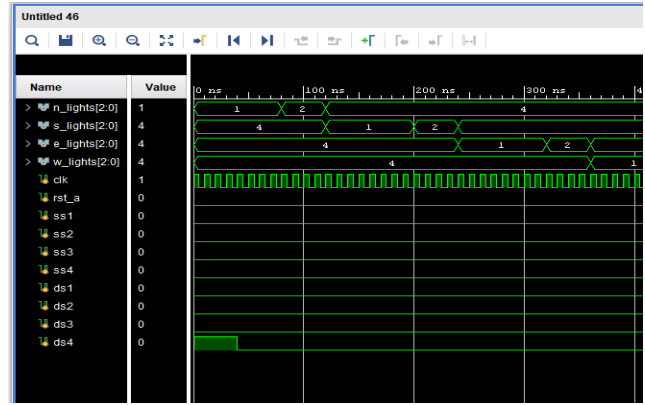


Fig.8. Case 6 simulation results

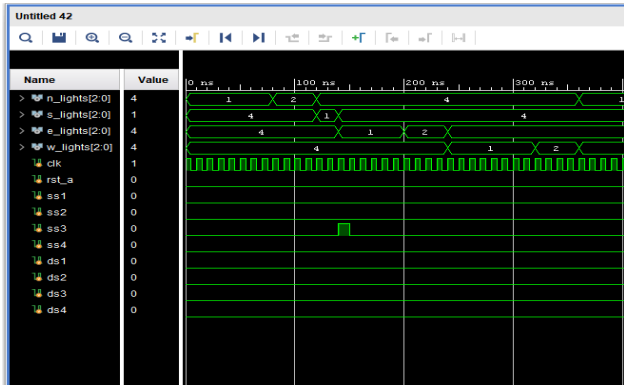


Fig.5. Case 3 simulation results

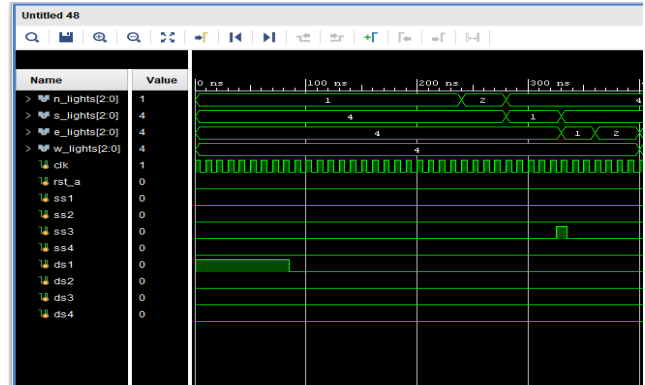


Fig.9. Case 7 simulation results

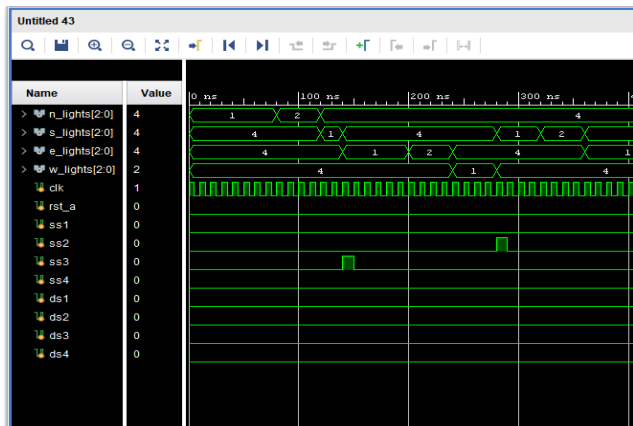


Fig.6. Case 4 simulation results

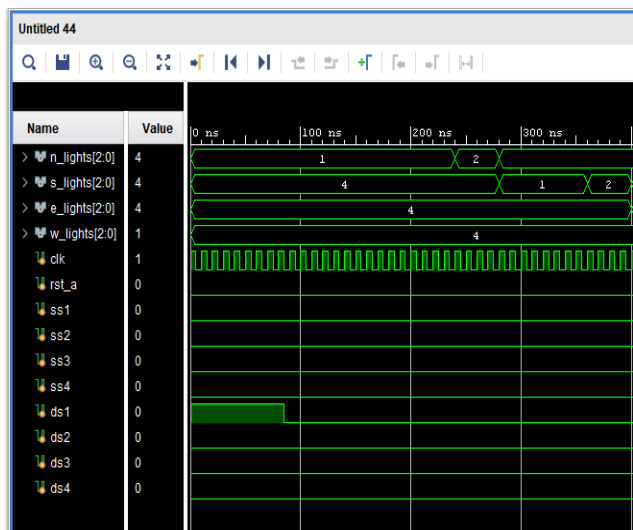


Fig.7. Case 5 simulation results

The following table 1 lists the hardware utilization on FPGA to implement the smart traffic controller logic:

Hardware	TOTAL LUTs	LOGIC LUTs	FFs
Utilization	15	15	7

The Fig.10. depicts that the power consumption is 3.118W from the device:

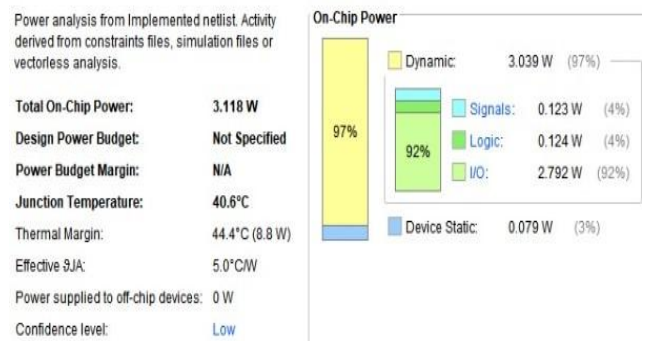


Fig.10. Power Consumption.

## V. CONCLUSION

An smart traffic controller is simulated which works with a normal counter moving green light to adjacent sides whilst others are red. Priority is given to ambulance, in case detected the particular line is made and the ambulance is allowed to pass. And also if density on one of the sides is more the time of green light is increased to clear the traffic. Further the data from the sensor can be recorded and stored in cloud. This data can be used to analyse the traffic density in the area.

The sensor can communicate to the FPGA via wireless modes by connecting a transmitter module to the sensor and receiver module to FPGA. The FPGA can be programmed to control the pedestrian lights as well.

## REFERENCES

1. W M El-Medany, M R Hussain, "FPGA-Based Advanced Real Traffic Light Controller System Design", IEEE international Workshop on Intelligent Data Acquisition and Advanced Computing System: Technology and Applications 6-8 September 2007, Dortmund, Germany.
2. Parasmani, Shri Gopal Modani, " FPGA-Based Advanced Traffic Light Controller Simulation", International Journal of Scientific & Engineering Research, Volume 4, Issue 9, September-2013.
3. "FPGA Implementation of an Advanced Traffic Light Controller using Verilog HDL", Dilip, Y. Alekhya, P. Divya Bharathi, Advanced Research in Computer Engineering & Technology; Volume 1, Issue 7, pp: 2278 – 1323, 2012.
4. Z. Yuye and Y. Weisheng, "Research of Traffic Signal Light Intelligent Control System Based On Microcontroller," 2009 First International Workshop on Education Technology and Computer Science.
5. Taehee Han; Chiho Lin, "Design of an intelligence traffic light controller (ITLC) with VHDL," Proceedings 2002 IEEE Region 10 Conference on Computers, Communications, Control and Power Engineering (TENCON '02), 28-31 Oct. 2002, vol 3, pp:1749 - 1752
6. "FPGA-Based Advanced Real Traffic Light Controller System Design". El-Medany, W.M. ; Univ. of Bahrain, Sakhr Hussain, M.R. DOI:10.1109/IDAACS.2007.4488383 Publisher: IEEE.

## AUTHORS PROFILE



**Sowmya K B** received the B.E degree in Electronics and Communication Engineering from the Vivekananda College of Engineering and Technology, Puttur, India, in 2006, M.Tech degree in Electronics from the Sir. M. Visveswaraya Institute of Technology, Bengaluru, India, in 2012, bagging rank from VTU, Belagavi. She was working as Assistant Professor in PA College of Engineering, Mangaluru, India for Nine years. Currently she is working as Assistant Professor in R V College of Engineering, Bengaluru, India. Her research interests include VLSI and Signal Processing, Image processing, Low power Architectures and VLSI Design. She has contributed many National and International journals to various reputed journals and conference .



**Sagar T** is Bachelor of Engineering degree pursuing student from the R V College of Engineering, Bengaluru. He predominantly works in the field of VLSI and Artificial Intelligence. His research interest is in the field of Neuromorphic systems.



**N.R Pavan Santosh** is Bachelor of Engineering degree pursuing student from the R V College of Engineering, Bengaluru. He predominantly works in the field of VLSI and Artificial Intelligence.