

FPGA Implementation in Robust FFT Architecture for Signal Processing Applications

L.Malathi, A.Bharathi, A.N.Jayanthi



Abstract—FFT architecture is the common and very efficient design in modern signal processing applications. Though so much of architectures are executed in now-a-days applications, This paper will give different approach of FFT design. In order to reduce the computation time, FFT structure is modified in the arrangement. This analyzed approach somewhat satisfies the low power, high performance and to useful in image, signal and wireless applications.

Keywords—FFT, Scaling Factor, Multiplier, CSA, CLA, BM, AM

I. INTRODUCTION

FFT is basically a composition of mathematical analysis. In an invariant approach transformation will estimate the scaling and rotation components. In FFT computation multipliers are play the major role. In the proposed approach there is research is done with the multipliers with the existing results which has done already. Throughout this proposal the high consideration in multipliers and adders used in FFT architecture.

II. METHODOLOGY

A. Survey on FFT Methodology

X(k) is the transformed version of x(n) is mathematically given as,

$$X(k) = \sum_{n=0}^{N-1} x(n)e^{-i2\pi nk/N}, \quad k = 0, 1, \dots, N-1 \quad (1)$$

$$X(k) = \sum_{n=0}^{N-1} x(n)W_N^{nk}, \quad k = 0, 1, \dots, N-1 \quad (2)$$

Scaling factor for N as common,

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$$W_N = e^{-i2\pi/N} = \cos\left(\frac{2\pi}{N}\right) - i \sin\left(\frac{2\pi}{N}\right) \quad (3)$$

$$W_N^{mN} = \left(e^{-i2\pi/N}\right)^{mN}, \quad m = -\infty, \dots, -1, 0, 1, \dots, \infty = e^{-i2\pi m} = 1. \quad (4)$$

IFFT of X(k) is mathematically given as,

$$x(n) = \frac{1}{N} \sum_{k=0}^{N-1} X(k)e^{i2\pi nk/N}, \quad n = 0, 1, \dots, N-1 = \frac{1}{N} \sum_{k=0}^{N-1} X(k)W_N^{-nk}, \quad n = 0, 1, \dots, N-1. \quad (5)$$

$$X(k) = \sum_{n=0}^{N-1} x(n)W_N^{nk}, \quad k = 0, 1, \dots, N-1 = W_N = e^{-i2\pi/N} \quad (6)$$

$$X(k) = \sum_{n_{\text{even}}=0}^{N-2} x(n)W_N^{nk} + \sum_{n_{\text{odd}}=1}^{N-1} x(n)W_N^{nk}. \quad (7)$$

When implement further we get,

$$X(k) = \sum_{m=0}^{N/2-1} x(2m)W_N^{2mk} + \sum_{m=0}^{N/2-1} x(2m+1)W_N^{(2m+1)k} = \sum_{m=0}^{N/2-1} x(2m) (W_N^2)^{mk} + \sum_{m=0}^{N/2-1} x(2m+1) (W_N^2)^{mk} W_N^k. \quad (8)$$

Scaling factor is,

$$W_N^2 = \left(e^{-i2\pi/N}\right)^2 = e^{-i2\pi 2/N} = e^{-i2\pi/(N/2)} = W_{N/2}. \quad (9)$$

Scaling factors actually drive the entire system of FFT throughout from input to output. Hence, delay also an impact on the implentaion result. By analysing the timing behaviour of the scaling factor implementation result will be under on an expected circle.

$$\begin{aligned}
 X(k) &= \sum_{m=0}^{N/2-1} x(2m)W_{N/2}^{mk} + W_N^k \sum_{m=0}^{N/2-1} x(2m+1)W_{N/2}^{mk} \\
 &= \sum_{m=0}^{N/2-1} x_{\text{even}}(m)W_{N/2}^{mk} + W_N^k \sum_{m=0}^{N/2-1} x_{\text{odd}}(m)W_{N/2}^{mk}, \\
 &k = 0, 1, \dots, N-1
 \end{aligned}
 \tag{10}$$

$$X(k) = \text{DFT}_{N/2} \{x_{\text{even}}(m), k\} + W_N^k \cdot \text{DFT}_{N/2} \{x_{\text{odd}}(m), k\}
 \tag{11}$$

$$\begin{aligned}
 W_N^{x+N/2} &= W_N^x W_N^{N/2} \\
 &= W_N^x \left(e^{-i2\pi/N} \right)^{N/2} \\
 &= W_N^x e^{-i2\pi N/2N} \\
 &= W_N^x e^{-i\pi} \\
 &= -W_N^x.
 \end{aligned}
 \tag{12}$$

$$\begin{aligned}
 X(0) &= x(0) + x(1) \\
 X(1) &= x(0) - x(1).
 \end{aligned}
 \tag{13}$$

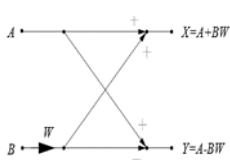


Fig. 1 Radix-2 Butterfly Structure

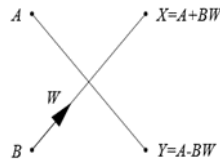


Fig.2 Simplified Radix-2 Butterfly Structure

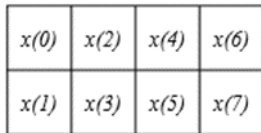


Fig.3 2-D approach of Radix-2 Structure

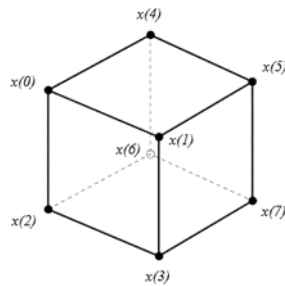


Fig.4 3-D approach of Radix-2 Structure

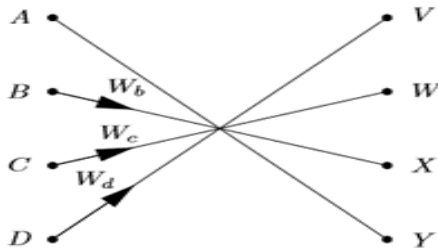


Fig.5 Radix-4 Butterfly Structure

Fig.1 and 2 shows the Radix-2 butterfly structure. Both structures are same but arrangement is different.

Three dimensional and two dimensional approach is implemented in FFT structure as shown in Fig.3 and Fig.4.

The outputs are,

$$\begin{aligned}
 V &= A + BW_b + CW_c + DW_d \\
 W &= A - iBW_b - CW_c + iDW_d \\
 X &= A - BW_b + CW_c - DW_d \\
 Y &= A + iBW_b - CW_c - iDW_d.
 \end{aligned}
 \tag{14}$$

In Eqn. (14) V,W,X,Y are the outputs. V is the addition of A,B,C,D. With B,C,D scaling factor is multiplied. In this step error tolerant multiplier approach is used. Her in order to eliminate the error truncated structure is implemented.

$$\begin{aligned}
 B' &= BW_b \\
 C' &= CW_c \\
 D' &= DW_d,
 \end{aligned}
 \tag{15}$$

Truncated outputs of B,C,D is given in Eqn. 15. Likewise W,X,Y is implemented, In between adders and subtractors are used. In the adder adder design selectors used to choose adder and subtractor.

$$\begin{aligned}
 V &= A + B' + C' + D' \\
 W &= A - iB' - C' + iD' \\
 X &= A - B' + C' - D' \\
 Y &= A + iB' - C' - iD'.
 \end{aligned}
 \tag{16}$$

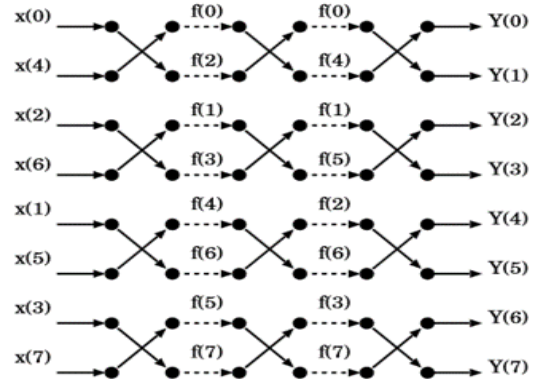


Fig. 6 FFT (8-Bit)

Table. 1 Comparison of FFT Radix

FFT Radix	Number of Complex Multiplications Required
2	0.5000 MN - (N - 1)
4	0.3750 MN - (N - 1)
8	0.3333 MN - (N - 1)
16	0.3281 MN - (N - 1)

Table. 2 Comparison of FFT with 'N'

Transform length (N)	DFT operations	FFT operations	DFT ops ÷ FFT ops
16	256	64	4
128	16,400	896	18
1024	1.05 × 10 ⁶	10,240	102
32,768	1.07 × 10 ⁹	4.92 × 10 ⁵	2185
1,048,576	1.10 × 10 ¹²	2.10 × 10 ⁷	52,429

From the table.2 according to N when DFT needs 256 operations, 64 operations as reduced in FFT. If N increases comparatively operations of FFT is reduced than DFT. In according with that the speed is a factor with increasing of N value. The speed in connected parameter with timing. In the proposed structure timing analysis done by in between each node in the entire structure.

Table. 3 Comparison of FFT with

N	FFT Radix	Real Multiplies Required	Real Additions Required
256	2	4096	6144
256	4	3072	5632
256	16	2560	5696
512	2	9216	13,824
512	8	6144	12,672
4096	2	98,304	147,456
4096	4	73,728	135,168
4096	8	65,536	135,168
4096	16	61,440	136,704

Power and Delay analysis of FFT in MOS,

$$P_{Total} = P_{Short-Circuit} + P_{Leakage} + P_{Switching} + P_{Constant-Current} \tag{17}$$

$$P_{switching} = C_{load} V_{dd}^2 f W \tag{18}$$

$$P_{switching_{node}} = a C_{load} V_{dd}^2 f W \tag{19}$$

$$C_{total} = C_{gate} + C_{diffusion} + C_{interconnect} \tag{20}$$

$$Delay \approx C_{total}/I \tag{21}$$

B. Review on Multipliers

Multipliers have large area and large propagation delays and thereby consume power. Therefore, Reduction in multiplications will give high impact on throughput of FFT output. For that different multipliers were reviewed. In that some multiplier approach is used to calculate the FFT.



Fig. 7 Reduction

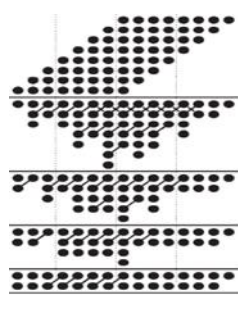


Fig. 8 Reduction Method 2

Error tolerant multiplier design shown in Fig.9 which depicts that, it includes two different multiplier connected as

parallel manner for MSB and LSB of input. The product also out from the respective multipliers.

An 8-Bit Multiplier Urdhva Tiryakbhyam Sutra is shown in Fig.10 to implement FFT. In that four 2-bit multipliers are connected in parallel manner. For this input is connected as bit serial order. The parallel outputs P0 to P7 out from the architecture.

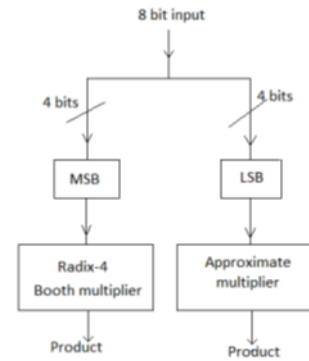


Fig.9 Error Tolerant Multiplier Design

For and addition carry look ahead adder is used. In Fig.11 Look Ahead approach is depicted. In the X(k) the output of FFT, the carry bypass adder is implemented as shown in Fig. 12 in order to bypass the carry out. In Fig.11 First level three AND gates are used to bypass the input to the next level. In second level half adder is used to originate the output. In carry bypass adder eight full adder is used.

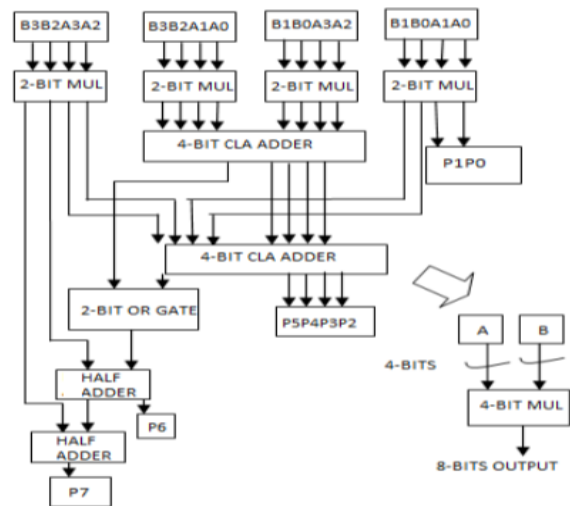


Fig.10 An 8-Bit Multiplier Urdhva Tiryakbhyam Sutra

C. Review on Adders

Adders are the basic unit in multipliers for high accuracy. If the performance of the multiplier is analyzed based on adders, then the other parameters can obtained as per designers requirement.

Here some of the topologies were analyzed according to VLSI approach (i.e.). Proposed adder is suited in different approach.

$$G_i = A_i \cdot B_i \quad \text{for } i=0,1,2,3 \quad (22)$$

$$C_i(\text{cout}) = G_i + P_i C_{i-1} \quad (23)$$

$$S_i = A_i \oplus B_i \oplus C_{i-1} \quad (24)$$

Eqn.22 gives the product of input A and B. $i=0,1,2,3$. Eqn. 23 and 24 gives sum and carry respectively.

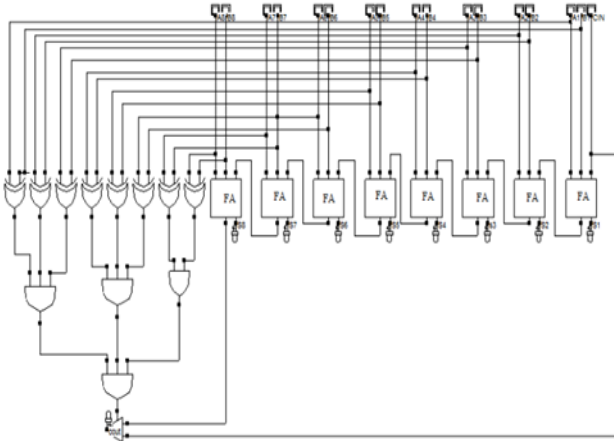


Fig. 11 Look Ahead Approach of Adder

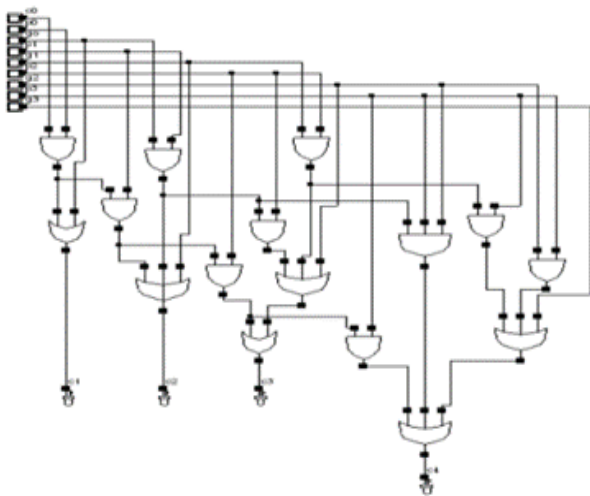


Fig.12 Carry Bypass Adder

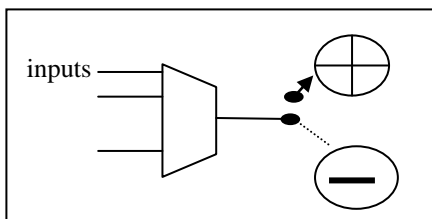


Fig. 13 Selection of Addition or

III. PROPOSED STRUCTURE AND DESIGN ANALYSIS

Optimized proposed here is, [Elisardo Antelo] Low Latency, Reduce Area and Delay, 34x34-digit Multiplication, Area:(20-35)%, [Xiaoxiao Zhang] Reduced Area and Power Consumption, For 32x32 bit,Area:11.1%, [Kostas Tsoumanis] Reduce the Critical Delay, Hardware Complexity and Power Consumption. Power: 2.30%-5.66%,Area: 2.16% - 10.85%, [Shin-Kai Chen] Reduce the Critical Path, Low Latency, [Artur K] Reduced Area, High Speed and High Accuracy, For 16X16-Bit Multiplier,Area:11.4%-25.4%, Reduced Latency and Delay,Latency:447Ps@2.5mV [Reza Azarderakhsh] Reduce the Latency, Reduce Area and Time Delay at Different Digit Sizes, High Speed Computation,By Using AISC and FPGA at Different Digit Size,Reduced Area & High Accuracy,DT Multiplier Error Reduced (87%, 16x16),Transistor Count is reduced by 47%.

A. Simulation Summary

Simulation results from the proposed structure is having acceptable rate of area, delay and power is reduced.

IV. RESULTS

A. Simulation Results

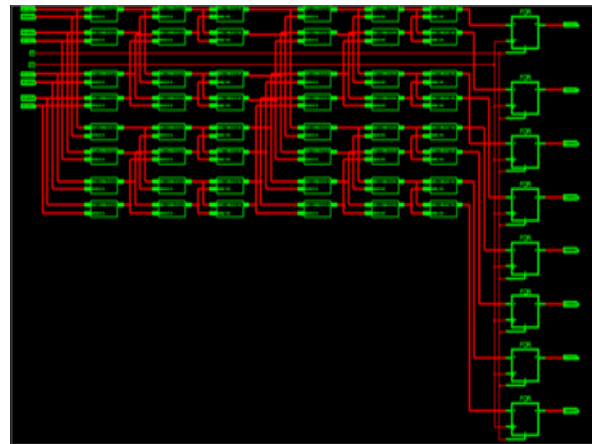


Fig.14 FFT Schematic

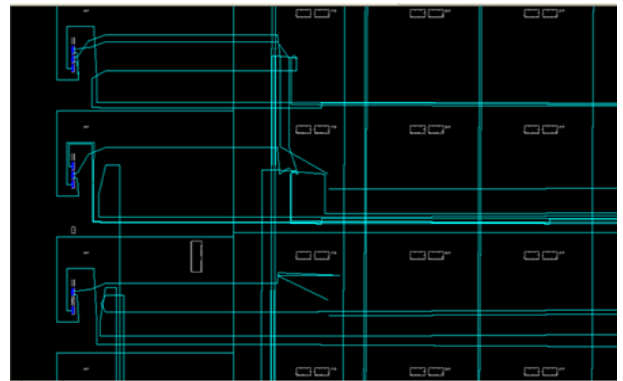


Fig.15 FPGA View -

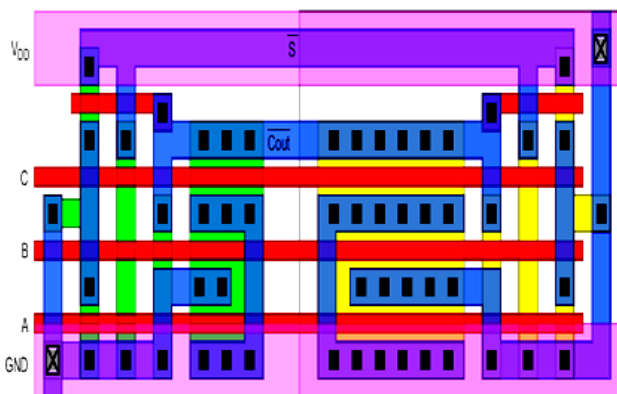


Fig.16 Layout – Adder

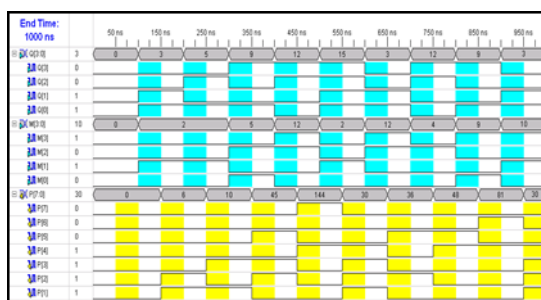


Fig.17 Simulation Result - Adder

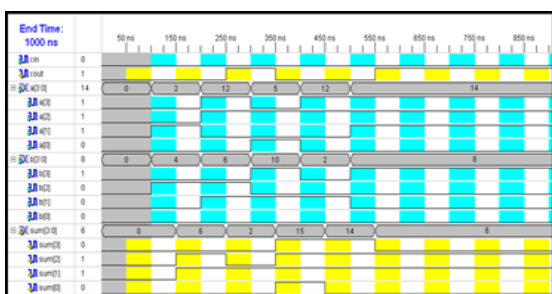


Fig.18 Simulation Result - Multiplier

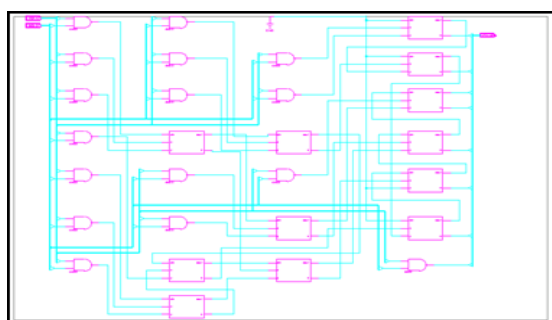


Fig.19 Schematic Multiplier

V. DISCUSSION

Based on the proposed architecture is some of the implementation discussions have to do by applying in finite response structures and multiplier based applications with an increasing bit rate.

VI. CONCLUSION

New dynamic data scaling architecture for pipeline FFT/IFFT have been proposed for 1-D applications. Based on fixed point pipeline low memory and arithmetic requirements have been constructed. This FFT/IFFT structure can be implemented in OFDM applications as Modulation/ Demodulation in communications for high signal quality. High throughput outputs have been obtained and scaling of data stalling has been avoided when data is continuously streaming by using pipeline architecture. Instead of DFT, in this project FFT is proposed for speedup the computations. In FFT/IFFT computation, if we increase the size of word length, quality of the signal and the throughput will automatically increased.

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