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Implementation of 16bit Fully Parallel Polar Encoder and Decoder using Partially Parallel Register Less Technique

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Abstract: ***This paper is about implementation of fully parallel polar encoder and decoder using partially parallel register less technique. Internal architecture consists of register less partially polar encoders and decoders. Compared to fully parallel polar encoder and SC polar decoder, proposed design has less area and less power consumption. Implementing long polar codes using fully parallel polar encoder and decoder is complex. In such cases proposed design can be used. Polar codes having simple structures and good performance. Proposed design is implemented using Synopsis. Simulation process is done in VCS and Xilinx. Polar codes widely used in 5G technology, these are the codess for control channels in 5G standard.***

Keywords: Register less Polar Decoder, Register less Polar Encoder, Verilog.

I. INTRODUCTION

Polar codes reached the channel capacity, they reduced complexity in encoding and decoding process. Polar codes are block codes. Linearity property holds good in polar codes. Polar codes having predominant applications in communication field as well as information storage devices. Polar codes implemented with short kernels. These short kernels undergo with multiple recursive concatenations. Due to this actual channel converted into artificial channels. The new artificial channels are polarized means each bit can be transmitted with different reliability and probability.so there is different probability for decoding. Even though polar codes have been idea about being with low complexity, they will experience problems like more hardware complexity and long inactivity compared to the best channel codes. Polar encoding is more vigorously used ascribable to the attaining channel property. Polar codes are strong contender to provide ultimate performance everybody needs in 5G communication system and focusing on coding methods in 5G are particularly polar codes and LPDC codes. Polar codes are sequential in nature.

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Error correcting performance of polar codes is best, in case of lengthy codes compared to LPDC codes. Polar codes implemented in 5G technology as error control codes. Encoding and decoding architectures of polar coding are implemented previously [1]-[5].
If folded transformation implemented on polar codes [8] we need more registers to store the intermediate data. In this paper fully parallel polar encoder and decoders are implemented with register free partially polar encoders and decoders. Proposed design has less power consumption and less area compared to fully parallel polar encoder and SC decoder. Proposed design can be extended for long polar codes also.

II. WORKING ARCHITECTURE

Fully parallel polar encoding and decoding is difficult to implement for long polar codes due to number of gates and more memory size. Even though fully parallel polar encoder and SC decoder achieving good error correcting performance, in fully parallel architecture 32 XOR gates are used as show in figure1 for 16-bit code. Polar codes have the simple structures and implemented with polar transform which is invertible transform. Polar codes which has length N. number of stages n, n=2^n, coding complexity O (N$\log N$). At each stage code is knocker's product of matrix $\begin{bmatrix}1 & 0\\ 1 & 1\end{bmatrix}$ which is kernel for polar transform. Polar codes implemented using generator matrix(kernel) in recursive definition. Combining and splitting of channel causes polarization. Due to this polarization process channels divide into perfect and noisy. Transmitting of information will be done through perfect channels and bits in noisy channel are frozen. Any power of two there is a polar transform. Polar codes are block code having linearity property Folding is the concept which is used in DSP. It is very helpful in reducing number of functional blocks in the design. The main disadvantage is we need more memory elements and multiplexers. In the existing register less partial encoder and decoders, giving input and retrieving output data requires complex hardware circuitry such as 16-bit registers, frequency divider circuits and 4-bit registers. It has four stages as inputs moves stage by stage. In one clock cycle we can give only 4 bits at a time and need to wait code to complete 4 stages to give next 4bit input. Due to this, the number of clock cycles for giving input and retrieving output are more.

This problem is avoided in proposed architecture by sending entire 16-bit input in one clock cycle only. In proposed architecture register less encoding and decoding was done. In proposed encoder and decoder architectures, 16-bit input is divided into four 4bit vectors. It has four stages as inputs moves stage by stage.

At every stage code is transformed and generate symbols. These symbols act as code for next stage (property of linear block codes). In existing register less partially parallel architecture due to high delays, the proposed architecture is designed with four internal modules without registers. These internal modules combined through outer module as shown figure6 and figure7. Each internal module generates individual outputs as 4-bit arrays and finally get combined as 16-bit output through outer module. In the proposed architecture, complexity and delays are reduced. Proposed design uses one clock cycle only for execution, thus number of clock cycles for giving input and retrieving output are reduced. So, proposed design achieves less execution time when compared to the existing design. As code length is increased implementing fully parallel polar codes becomes complex. In these cases, proposed design can be implemented. Proposed design simulated using Xilinx and VCS tools.

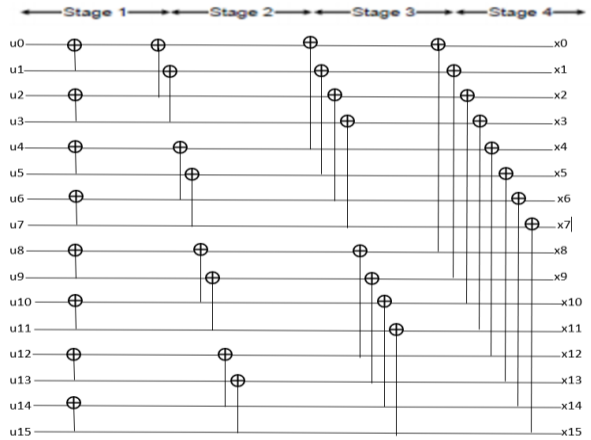

Fig. 1. Fully parallel Polar Encoder

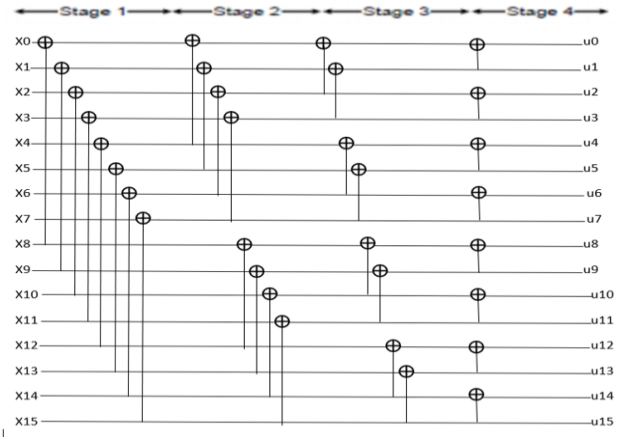

Fig.2. Fully parallel Polar SC Decoder

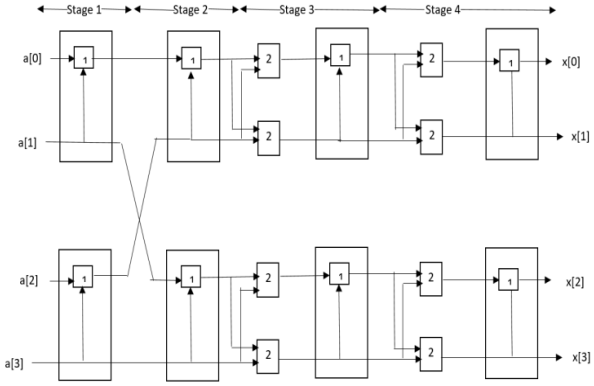

Fig. 3 4 bit register less polar encoder

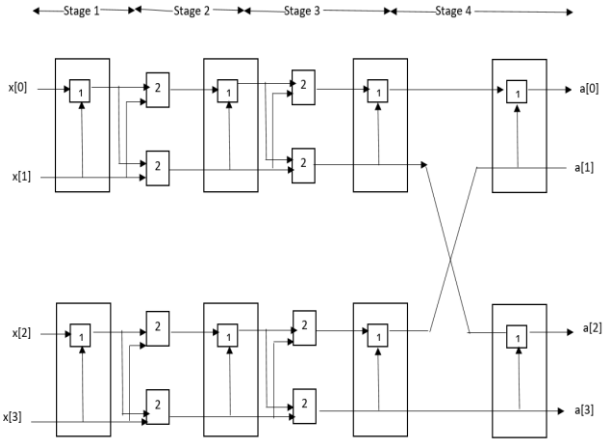

Fig. 4. 4 bit register less polar decoder

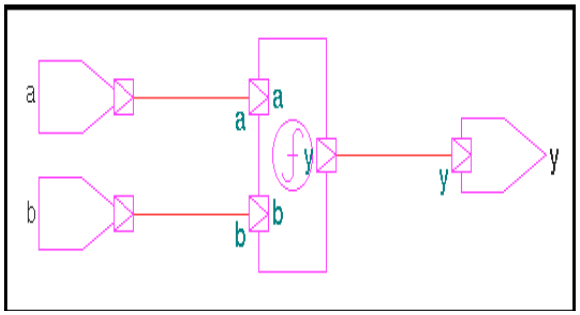

Fig. 5. Cell 1

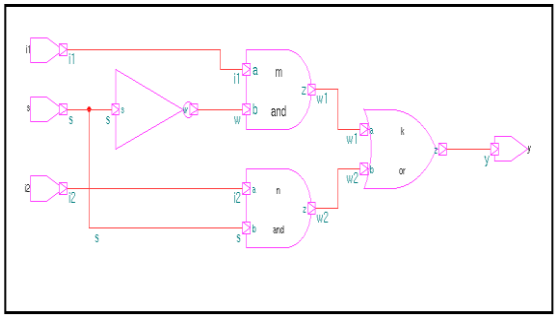

Fig. 6. Cell 2

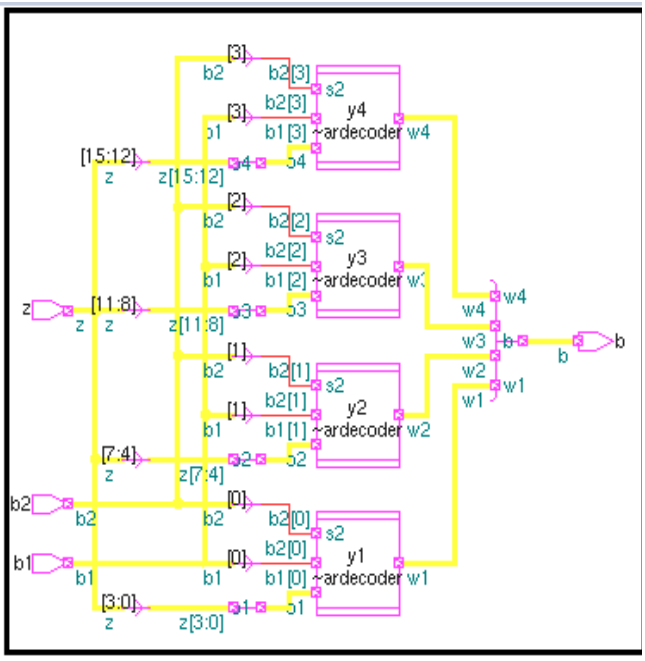

Fig. 7. 16 bit Advanced polar decoder

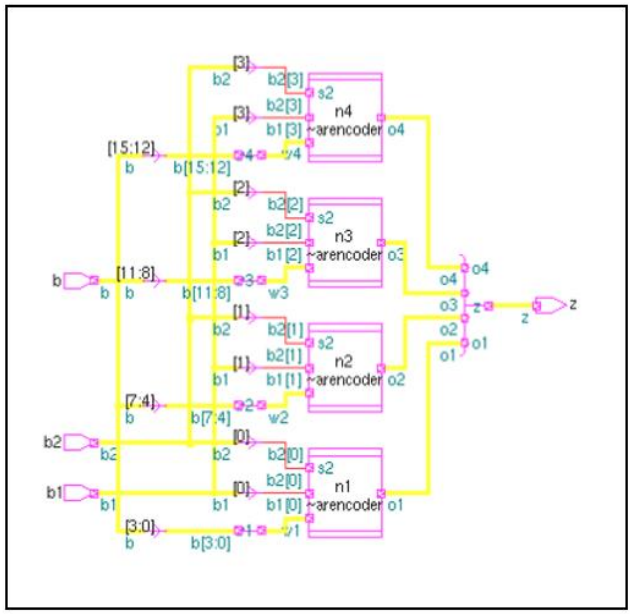

Fig. 8. 16 bit Advanced polar encoder

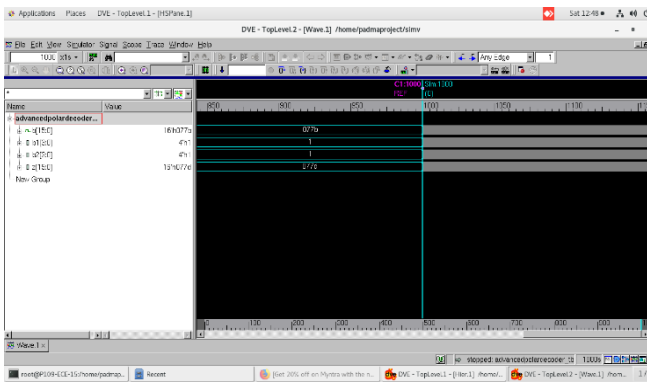

Fig. 9. VCS output - Advanced polar decoder

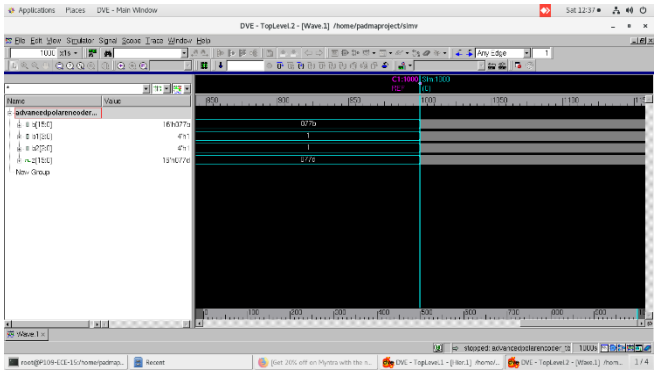

Fig. 10. VCS output - Advanced polar encoder

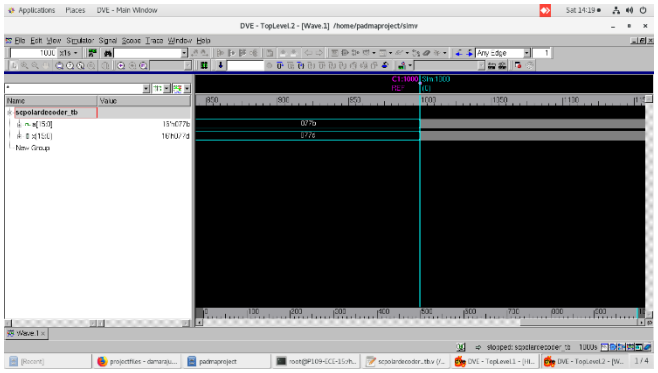

Fig. 11. VCS output - SC polar decoder

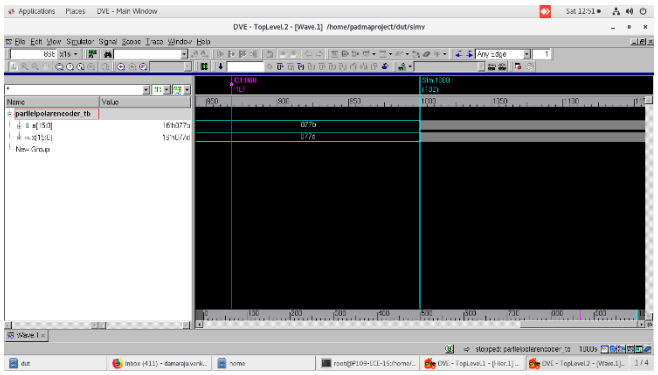

Fig. 12. VCS output - Fully parallel polar encoder

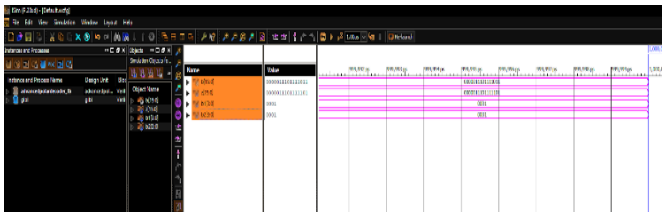

Fig. 13. Xilinx output – Advanced polar decoder

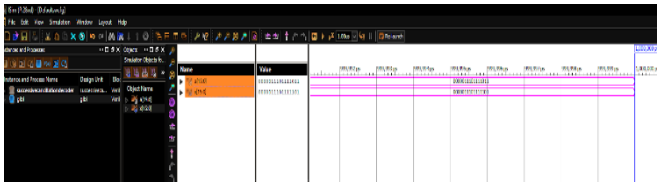

Fig. 14. Xilinx output – SC decoder

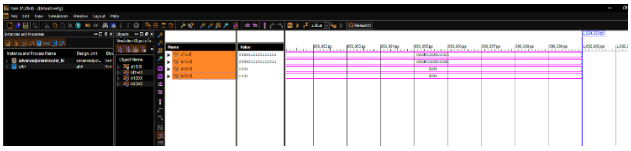

Fig. 15. Xilinx output – Advanced polar encoder

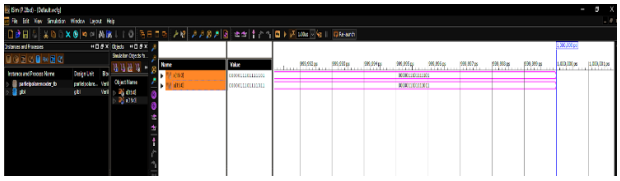

Fig. 16. Xilinx output – Fully parallel polar encoder

Table- I Achieved results with proposed design

	Compile time	Area	Dynamic power
Fully parallel polar encoder	0.36	428.54	193.2894 uw
16 bit advanced polar encoder	0.41	33.32	9.0192 uw
Fully parallel SC polar decoder	0.42	428.54	190.0783 uw
16 bit advanced polar decoder	0.44	33.32	9.0192 uw

Table- II comparison of proposed design with existing design

Terms	Existing Design	Proposed Design
Power	99 (mw)[13]	9.0 (uw)

III. CONCLUSION

In this paper, the proposed design achieved better performance in terms of power when compared with existing register less partially polar encoder and decoder architectures. Fully parallel encoder and SC decoder designed and compared with proposed architecture Using DC compiler. The proposed design achieved less area and less power consumption. Through this design, data transmission level of performance is improved. Thus, compared to fully parallel polar codes, the proposed design can be used for real-time lengthy polar codes.

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